96768550

CONTROL DATA CORPORATION

CDC® BUFFERED COMMUNICATION LINE ADAPTER

DT610, DY221, FJ127, FJ128

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
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REVISION RECORD

REVISION	DESCRIPTION
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(10/80)	
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(5/81)	
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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
AT391-A	01		
DT610-A	01		
DY221-A	01		
FJ127-A	02		
FJ128-A	01		

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV
Cover	--
Title Page	--
ii	D
iii/iv	D
v/vi	D
vii/viii	D
ix	A
x	C
1-1	A
1-2	A
1-3	C
1-4 thru 1-8	A
2-1 thru 2-16	A
3-1	A
4-1 thru 4-34	A
5-1 thru 5-50	A
5-51 thru 5-53	B
6-1	A
7-1 thru 7-24	A
7-25	B
7-26	B
7-27 thru 7-30	C
A-1	A
B-1 thru B-20	A
C-1 thru C-58	A
Comment Sheet	D
Cover	--

PAGE	REV

PAGE	REV

PAGE	REV

PAGE	REV

PREFACE

This manual describes the CONTROL DATA® FJ127-A Primary Buffered Communication Line Adapter and FJ128-A Expansion Buffered Communication Line Adapter, DY221-A Current Loop Adapter, and DT610-A Current Loop Expansion. These adapters utilize a combination of logic and firmware to accomplish their control functions. This manual contains general descriptions, operating procedures, theory of operation, and diagrams needed by programmers, operators, and customer engineers for the use and maintenance of the equipment.

The CDC publications listed below provide additonal information related to installation, operation, and maintenance of the adapter:

Publication	Publication Number
Basic Micro-Programmable Processor Hardware Maintenance Manual	39451400
Micro-Programmable Computer Family Micro Processor Hardware Reference Manual	88973400
CYBER 18 Computer Systems with MOS Memory Installation Manual	96768360
DT120, DT195, FC402 Breakpoint Controller and Breakpoint Panel Hardware Reference/Maintenance Manual	96729000
CYBER 18 Computer Systems Overview Manual	60475000
DT610, DY221, FJ127, FJ128 Buffered Communication Line Adapter Field Repair Guide	60475130

CONTENTS

APPENDIXES

FIGURES

TABLES

GENERAL DESCRIPTION 1

This section contains the physical and functional description of the multichannel asynchronous buffered communication line adapter (BCLA) to be used in CYBER 18 computer systems. The adapter provides up to 16 RS232-C (CCITT V.24) interfaces to a CYBER 18 processor. The complete adapter consists of the printed wiring assemblies (PWAs) that are installed in the processor and three cable harnesses. Functional control of the adapter is via microcode stored in read-only memory (ROM) on the primary PWA. Figure 1-1 shows a typical system block diagram.

The BCLA provides modem interface signals to permit operation with asynchronous modems in either half-duplex or full-duplex systems. Each port of the BCLA consists of a receive channel and a transmit channel; both channels may transfer data simultaneously. Available modem signals provided by the BCLA permit auto-answer/ auto-disconnect capability when used in conjunction with appropriate software and modems. Operation without modems in a local-terminal system is possible using either an RS232-C voltage interface or a Teletype-compatible, 20-milliampere current loop mode.

The equipment consists of the following major components:

- The primary printed wiring assembly
- The expansion printed wiring assembly
- Three wire harness assemblies
- Backplane-to-cable-harness adapters
- Optional current loop adapters

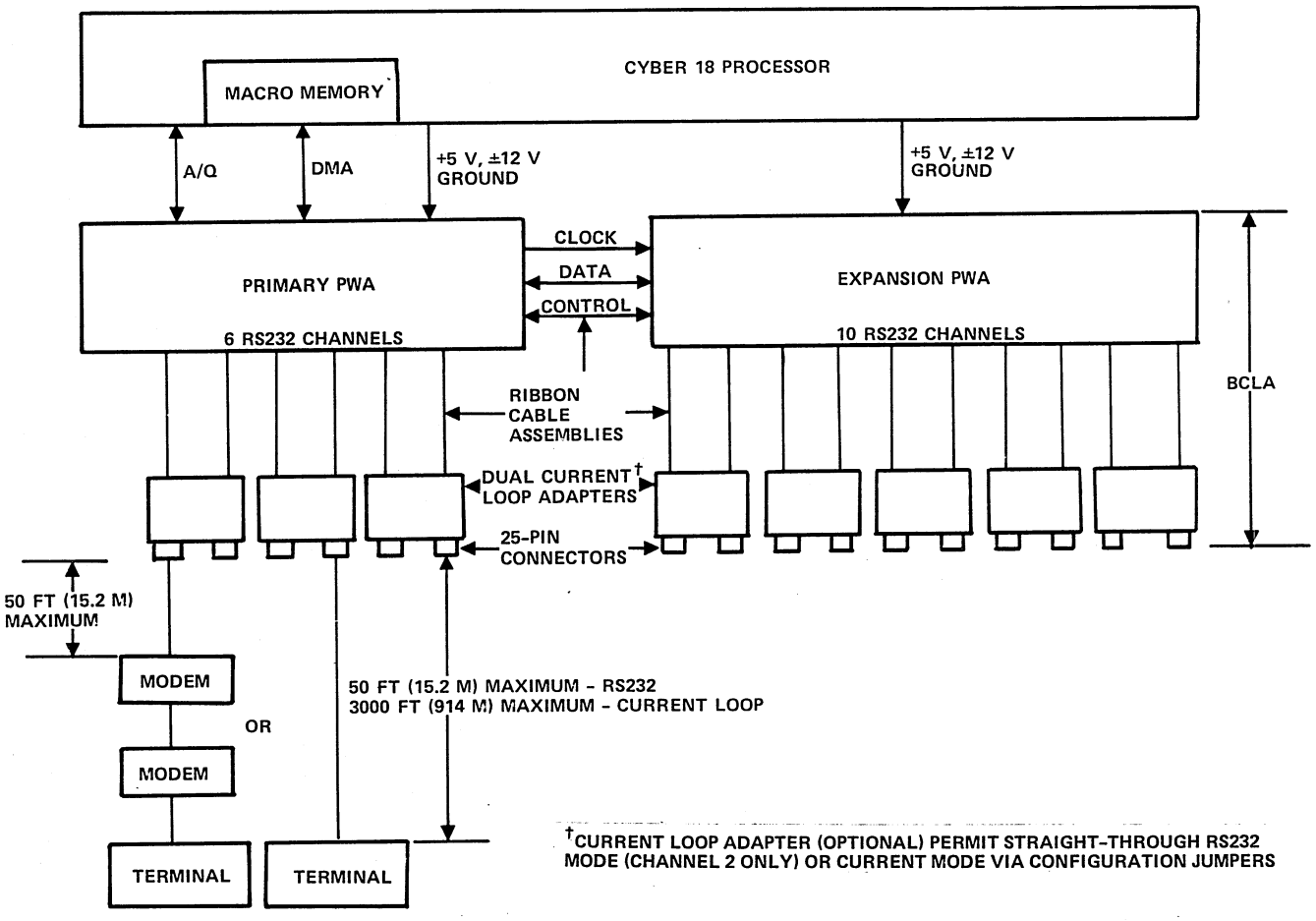


Figure 1-1. BCLA System Block Diagram

The primary printed wiring assembly may operate independently to provide a six-port BCLA. Both PWAs provide 16 asynchronous communication ports. Two complete BCLAs may be installed in one CYBER 18 Computer System.

PHYSICAL DESCRIPTION

PRIMARY PWA

The primary BCLA, figure 1-2, is a four-layer printed wiring assembly that measures 11 by 14 inches (279 by 356 millimeters). It contains capacitors, resistors, and integrated circuits that form the analog and transistor-transistor logic (TTL) circuits. These circuits produce the BCLA interface, control timing, firmware program, logic control, and data functions that control six communication channels and provide the read/write communication link between the communication channels and the central processor.

The primary BCLA is installed in one of the A/Q-DMA slots of the processor.

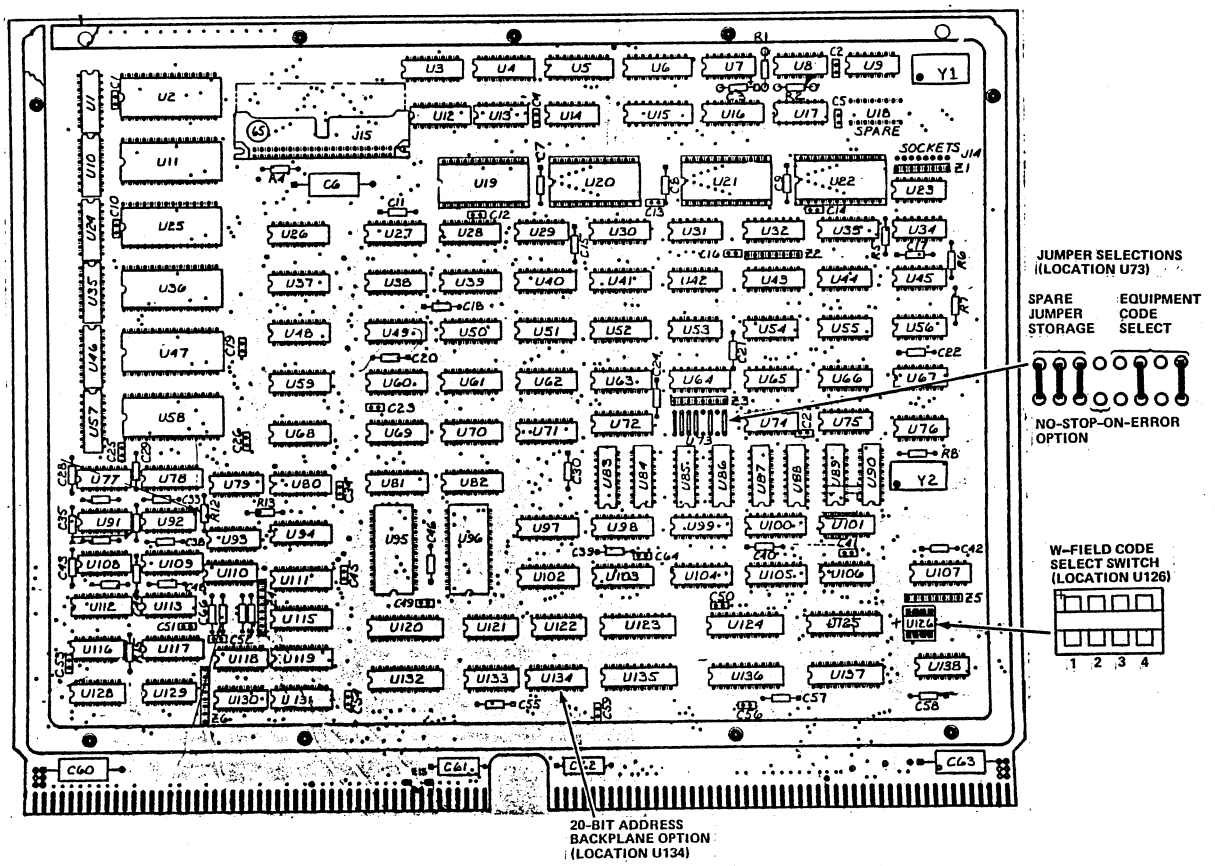


Figure 1-2. Primary BCLA Printed Wiring Assembly

EXPANSION PWA

The expansion BCLA, figure 1-3, is a printed wiring assembly that measures 11 by 14 inches (279 by 356 millimeters). It contains capacitors, resistors, and integrated circuits that form the analog and TTL circuits. These circuits provide the read/write communication link between ten communication channels and the primary BCLA. Logic control for the expansion PWA is provided by the primary PWA via a 40-conductor ribbon cable near the front edge of the two PWAs. The expansion BCLA is installed in one of the peripheral A/Q slots of the processor adjacent to the primary BCLA.

BACKPLANE-TO-CABLE-HARNESS ADAPTERS

The backplane-to-cable-harness adapters, figure 1-4, provide the interface between the PWA backplane connector and the RS232-C cable entry panel. The primary adapter accommodates six lines, and the expansion adapter accommodates ten expansion lines. The adapter, supplied with the applicable PWA, is installed over the processor backplane pins of the appropriate card slot.

WIRE HARNESS ASSEMBLIES

Three wire harnesses are associated with the BCLA and are supplied with the appropriate PWA. The primary PWA is supplied with one harness consisting of six ribbon cables. These cables provide the interface between the primary backplane-to-cable-harness adapter and six communication lines at the I/O connector panel located at the rear of the processor cabinet (the I/O connector panel is a required option of the BCLA).

The expansion PWA is supplied with two cable assemblies. One is a plug-in ribbon cable assembly that interconnects the primary and expansion PWAs. This cable is installed at the front edge of the PWAs. The cable slack is tucked between the two circuit boards to permit installation of the processor chassis cover. Also supplied with the expansion PWA is one harness consisting of 10 ribbon cables. These cables interface the expansion communication lines between the backplane adapter and the I/O connector panel.

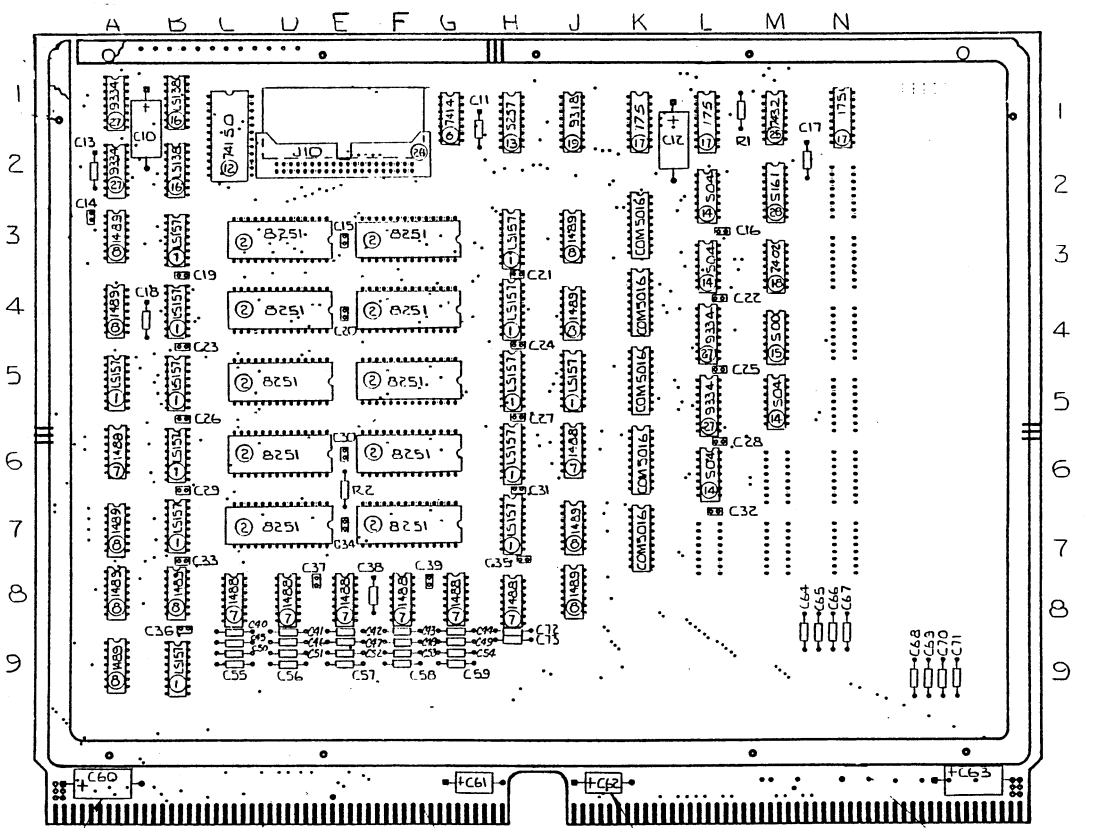


Figure 1-3. Expansion BCLA Printed Wiring Assembly

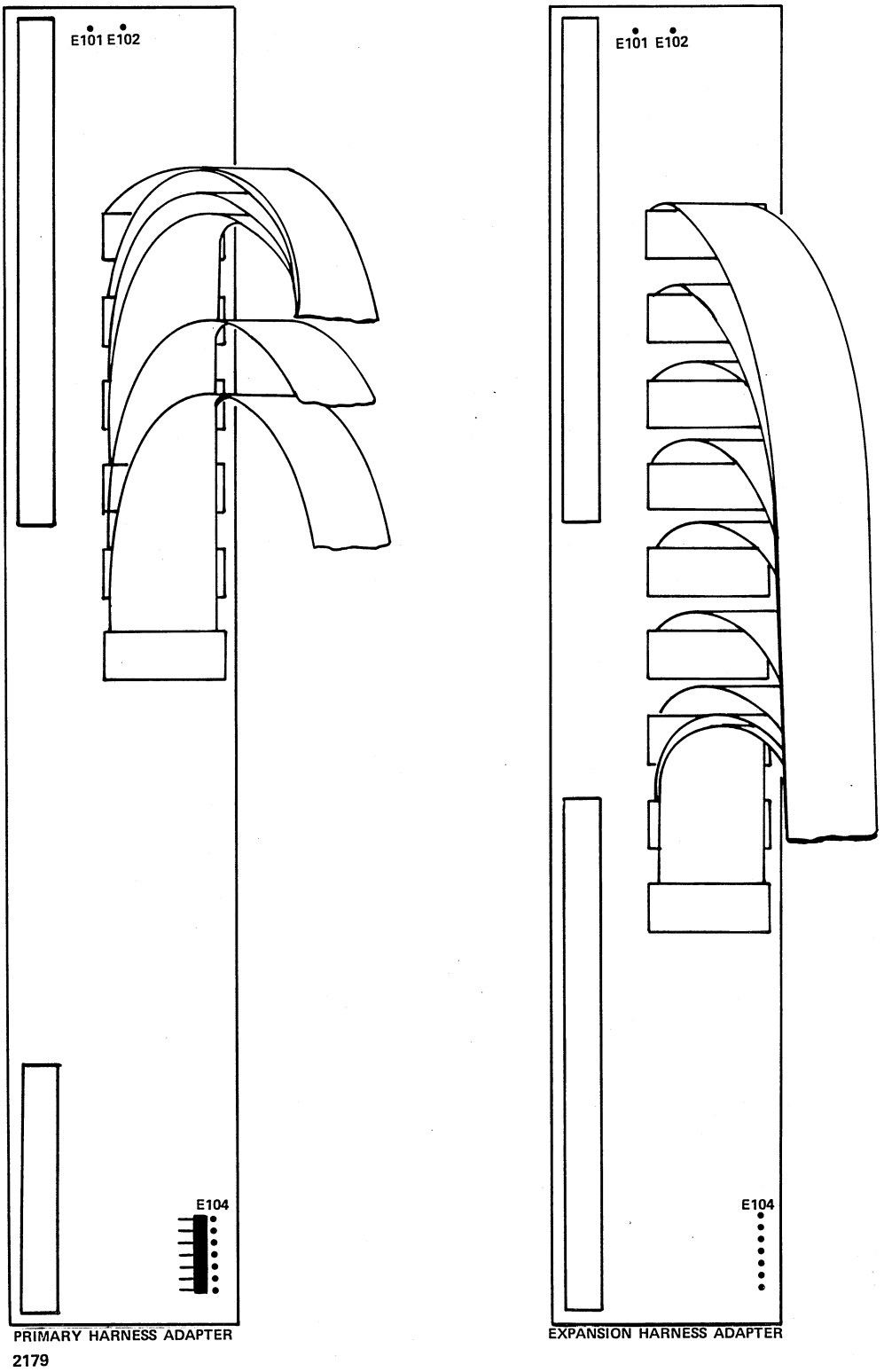


Figure 1-4. Backplane-to-Cable Harness Adapters

CURRENT LOOP ADAPTERS

Signals from the communication line must be RS232-C compatible at the I/O pins of the BCLA. To achieve this compatibility, industry-standard drivers and receivers are used between the TTL levels of the BCLA circuitry and the external cable.

The current loop adapter is a printed wiring assembly supplied with the necessary connectors; it is installed on the I/O connector panel in series with the BCLA and the external device cable. Figure 1-5 shows current loop adapter application.

An add-on +24 V dc power supply (battery) to be installed on the top of the I/O connector panel is required to support the current loop adapters. Additional +12 V dc and -12 V dc wiring is also required. All wiring is provided with the current loop adapter installation kits.

FUNCTIONAL DESCRIPTION

PRIMARY PWA

The primary buffered communication line adapter has been designed and constructed in two parts. One part contains logic circuitry that is common to many I/O controller applications. This part, enclosed by dotted lines in figure 1-2, is referred to as the common controller logic. The remainder of the controller contains logic that is peculiar to the specific controller application, in this case the BCLA.

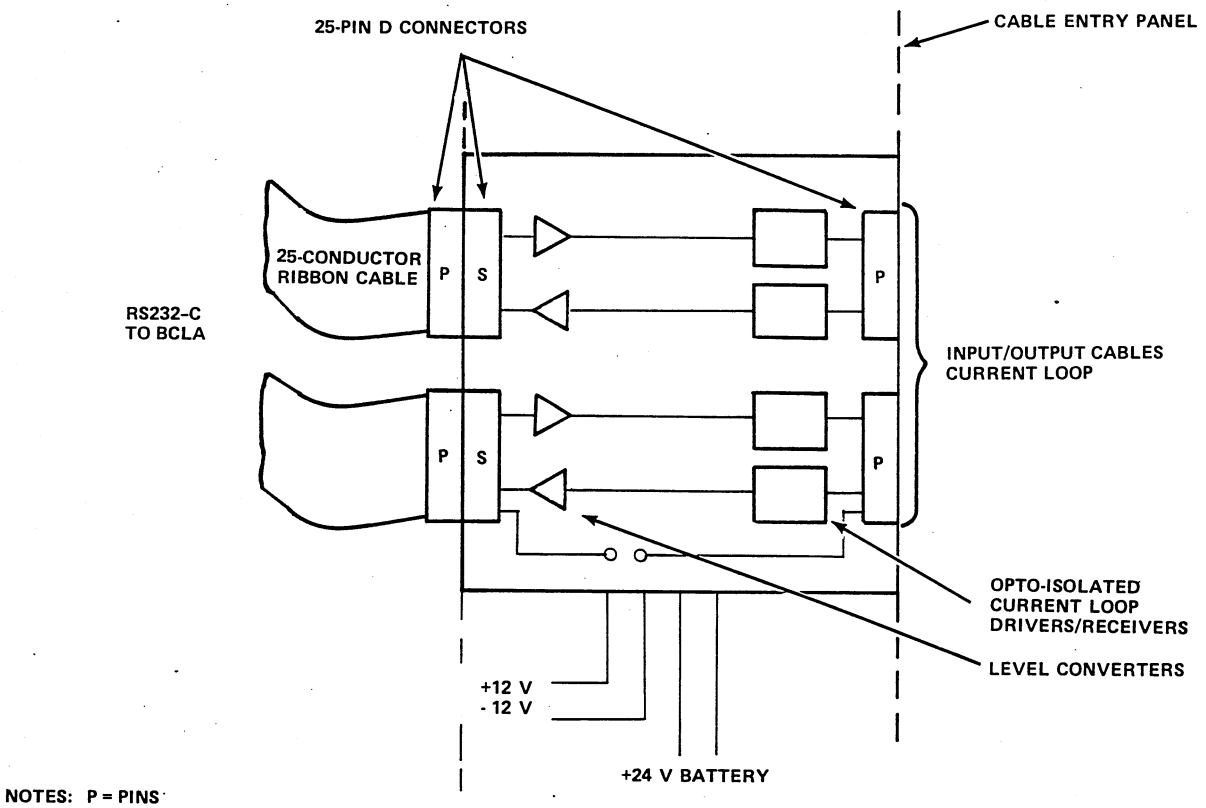


Figure 1-5. Current Loop Adapters and Level Converters

Common Controller

The common controller design centers around an eight-bit controller that is controlled by a firmware program contained in read-only memory (ROM) of 256 64-bit instruction words. The common controller (figure 1-6) contains two selectors, each consisting of a general-purpose register and multiplexer, a register file of 1, 024 eight-bit bytes, an arithmetic logical unit (ALU), and A/Q-DMA interface buffer registers that are controlled by the firmware (ROM) control fields. The ALU and firmware also provide data and control interface with the communication channel interface elements.

The common controller employs Schottky and regular TTL that provides execution of one instruction every 167 nanoseconds.

Communication Interface

The communication interface provides the link (data and control) between the common controller and the communication channels. The status of the channels is detected and coupled via the communication interface to the common controller to initiate the micro controller operation. Data bits from the active channels are serially shifted into the associated shift registers. These data bits are then parallel-loaded into the read buffer for transfer to the ALU via the selector.

Data and clock bits from the central processor unit (CPU) to the communication channels are transferred via the common controller selector and ALU bits for parallel loading into the write buffer. The write buffer contents are then parallel-transferred to the shifter, where the data bits are serially shifted to the active channel.

The communication interface consists of six data communication ports, all of which have identical characteristics. Each port is addressed by its own, unique, four-bit port number. Each port is operated independently in either transmit mode, receive mode, or both receive and transmit simultaneously (full duplex). The receive and transmit channels of any one port share a common set up (that is, baud rate, stop bits, character length, and so forth). Each port may be independently programmed for a specific operating mode.

In operation, all six transmitters and all six receivers contend for service from the micro processor section of the BCLA common controller. A transmitter requires service whenever it has shifted out a data character to the communication line. The micro processor must supply the transmitter with the next character. A receiver requires service whenever it has shifted in a data character from the communication line. The micro processor must empty the input buffer.

EXPANSION PWA

The expansion printed wiring assembly consists of ten data communication ports, all of which have characteristics identical to those of the ports of the primary communication interface. The expansion interface is merely an extension of the internal data, addressing, and control paths that originate on the primary PWA. This PWA is installed into an A/Q slot of the processor, but it uses only logic power and ground signals from the processor. The interface is implemented using the plug-in ribbon cable between the front edges of the primary and expansion PWAs.

CURRENT LOOP ADAPTERS

The optional current loop adapters are available for use with systems that require isolated data paths and are not RS232-C compatible. The adapter is designed to support remote terminal equipment. The adapter emulates the receive relay and transmit contacts found in terminal devices. The adapter conditions only transmit data and receive data signals. The modem control signals from the terminal are conditioned on the primary or expansion printed wiring assemblies.

The adapter is installed by inserting it in series with the BCLA ribbon cable and the external device signal cable at the I/O connector panel. Each adapter accommodates two data channels. One of the two circuits on the adapter may be bypassed by jumpers to permit normal RS232-C operation.

REFERENCE DATA

DATA TRANSFER RATES

Each port may be software programmed to transmit and receive at data transfer rates from 50 to 19,200 bits per second. In all cases, the receive and transmit clock rates for any one port are the same. Refer to section 2 for the rates that may be programmed.

CHARACTER TRANSFER AND BAND WIDTH

For any channel, the receiver and transmitter data transfer rates are the same. The maximum character transfer rate is 1,371 characters per second for both the receiver and transmitter during half-duplex operation or 2,743 characters per second during full-duplex operation. This rate is based on a programmed, five-bit data character with one stop bit and no parity for a total of seven bits. The BCLA maintains a data transfer rate of 9,600 bits per second based on a programmed, eight-bit data character with one stop bit and no parity. Refer to section 2 for character length and stop-bit programming requirements.

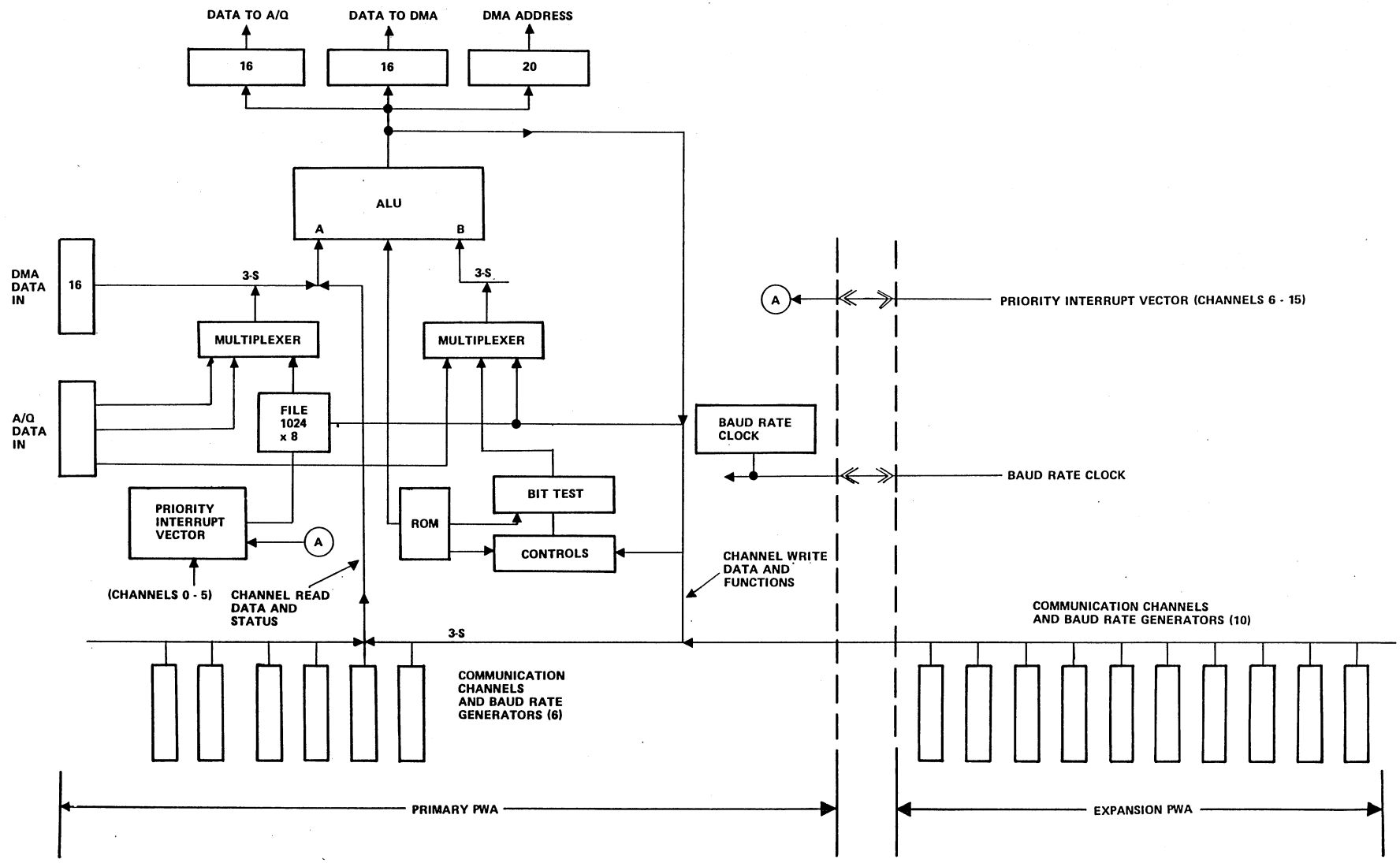


Figure 1-6. BCLA Functional Block Diagram

COMMUNICATION LINE CHARACTERISTICS

RS232-C Mode

All signal lines are to be RS232-C compatible. In order to achieve the voltage swings in excess of ±3 volts per RS232-C requirements, line drivers use the ±12 V dc power available from the processor backplane. The maximum ±12 V dc power supply current for one 16-channel BCLA is 0.5 amperes.

Current Loop Mode

The relationship of current loop current-to-voltage levels is as follows:

Loop Current	Line Condition	BCLA Logic
Flowing	Mark	1(+5 Volts)
Not flowing	Space	0(0 Volts)

The system current must be 20 milliamperes. The maximum open circuit system voltage may not exceed 24 volts, and the minimum open circuit system voltage is 10 volts. Maximum voltage drop across the transmitter (send contacts) circuit is 2 volts.

OPERATING ENVIRONMENT

The operating environment specifications are as follows:

Temperature - 40° to 120° F (4.5° to 49.0° C)

Humidity - 10 to 90 percent relative (no condensation)

Altitude - Sea level to 10,000 feet (3048 meters)

BCLA LOGIC LEVELS

The BCLA logic levels for Schottky and regular TTL are as follows:

Logic 0 (low)	0 to 0.4 volts
Logic 1 (high)	2.7 to 5.2 volts

OPERATION 2

This section contains descriptions of the controls and programming reference material for the buffered communication line adapter, including the primary and expansion printed wiring assemblies and the current loop adapter.

CONTROLS

One four-position dual inline package (DIP) switch at location U126 of the primary PWA (figure 1-2) and removable jumper plugs at locations U73 and E14 through E16 are used to establish operating addresses for the BCLA. Bits from the software program must match preset numbers for the BCLA to react to A/Q commands.

W-FIELD NUMBER SELECTION

The BCLA uses the four most significant bits of the Q register W field to identify individual BCLAs. Any W-field number from 1_{16} to F_{16} (binary 0001 to 1111) may be selected by the switch. Binary code 0000 is not a valid number for selection. Table 2-1 lists the relationship of Q bits to switch postions. A switch setting of on (closed) produces a logical zero on the BCLA that matches a logical one in the Q field.

EQUIPMENT NUMBER JUMPERS

An equipment number A_{16} (binary 1010) has been assigned for the BCLA in the CYBER 18 applications. This is established by inserting two jumper plugs at location U73 of the primary PWA. Figure 1-2 shows the proper jumper plug configuration.

NO-STOP-ON-ERROR OPTION

An optional no-stop-on-error bit is selected by one jumper plug at location U73 (figure 1-2) of the primary PWA. When the jumper is out (option not selected), the data transfer stops immediately if any error occurs. When the jumper is in (option selected), the data transfer is completed without stopping on the error. After completing the data transfer, the error is indicated in the termination status word. Refer to table 2-2.

20-BIT ADDRESS BACKPLANE

A jumper at location E14 to E16 (figure 1-2) is used with other configurations for the common controller portion of the PWA. A jumper is installed at this location when the controller is used in a CPU with 20-bit addressing capability. The jumper must not be installed when the BCLA is used in a CYBER 18 CPU with 18-bit addressing capability (normal configuration).

TABLE 2-1. W-FIELD NUMBER SELECTION

W-Field Address†† (Q15 through Q12)		Switch Position			
Hexadecimal Value	Binary Bits	1	2	3	4
0†	0000	Off	Off	Off	Off
1	0001	Off	Off	Off	On
2	0010	Off	Off	On	Off
3	0011	Off	Off	On	On
4	0100	Off	On	Off	Off
5	0101	Off	On	Off	On
6	0110	Off	On	On	Off
7	0111	Off	On	On	On
8	1000	On	Off	Off	Off
9	1001	On	Off	Off	On
A	1010	On	Off	On	Off
B	1011	On	Off	On	On
C	1100	On	On	Off	Off
D	1101	On	On	Off	On
E	1110	On	On	On	Off
F	1111	On	On	On	On

†The BCLA does not respond to any commands when the W-field switches (positions 1 through 4) are in the off position.

††The W field includes Q11; but since Q11 must always be zero, it is not shown on this table.

SPARE JUMPERS

The three remaining jumper points at location U73 (figure 1-2) of the primary BCLA are reserved for future development and storage of spare jumper blocks. Removal or insertion of jumpers in these points has no effect on BCLA operations.

TABLE 2-2. NO-STOP-ON ERROR OPTION SELECTION

Jumper Configuration	Option Selected
Out (normal mode)	Break or framing error and/or lost data error causes an immediate buffer terminate
In (special systems) application only)	Only a normal receive terminate is in effect (EOT or buffer length). Errors are reflected in the termination status word.

PROGRAM PROTECT

The BCLA always expects protected A/Q instructions. If program protect is not true (low), the BCLA rejects the command. This feature is a part of the BCLA construction, and no switch or jumper is required.

INTERRUPT WIRING

Each primary BCLA is capable of functioning as the master BCLA when multiple BCLAs are sharing the same macro interrupt line of the processor. Each primary BCLA generates an interrupt that is made available to the backplane at pin number 249, as shown in figure 2-1. This local interrupt is an active low state.

In systems that contain more than one primary BCLA, one must be designated as the master for the system. The interrupt line from pin 249 must be connected from the backplane of each primary BCLA, other than the master, to the master BCLA adapter board. Terminals E104 through E110 are located at the lower rear corner of the primary BCLA adapter board (figure 1-4). These terminals are used only on the master primary BCLA adapter board.

PRIMARY-TO-EXPANSION BCLA INTERFACE

The primary (six-channel) BCLA may operate independently in a processor direct memory access I/O slot. The expansion (ten-channel) BCLA plugs into an adjacent A/Q or unassigned slot and interfaces with the primary using a flat ribbon cable. The primary PWA does not know when an expansion PWA is in the system. Channel numbers are contiguous, with 0 through 5 for the primary PWA and 6 through 15 for the expansion PWA. The primary-to-expansion PWA interface is simply an extension of the internal data, addressing, and control paths that originate on the primary PWA.

PROGRAMMABLE OPERATING MODES

The following operating modes are software programmable on an individual channel basis. The modes are defined here and described in detail in the A/Q interface subsection.

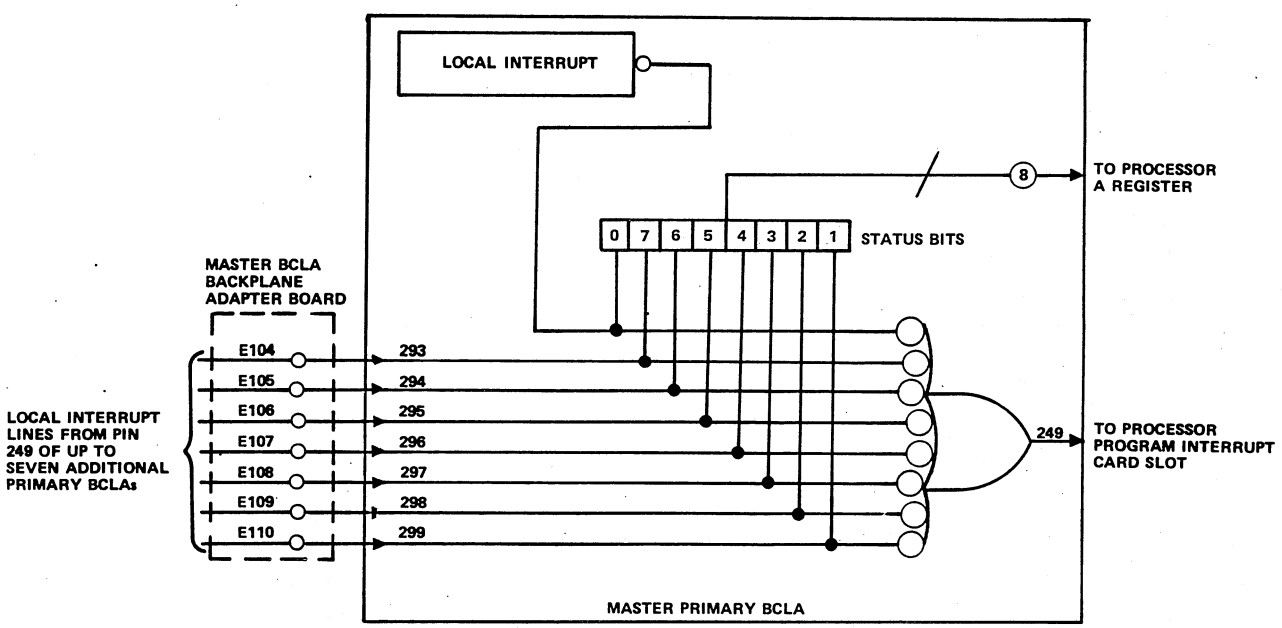


Figure 2-1. BCLA Interrupt Wiring

EOT CHARACTER

Software may operate in an open-end buffer mode when receiving data from a communication line. In this mode, the BCLA is programmable to terminate on one to ten end-of-text (EOT) characters. Each receive channel may be programmed with its own set of EOT characters. The BCLA terminates a receive operation whenever a character from the channel receiver is equal to a preset EOT character. Software must specify a buffer length to terminate a receive operation in the event that the EOT character is missed.

BAUD RATES

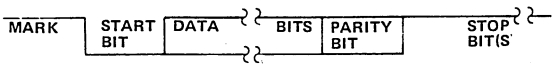
Each port may be software programmed to transmit and receive at one of the data transfer rates listed in table 2-3. In all cases, the receive and transmit clock rates are the same for any one port.

TABLE 2-3. TRANSFER RATE SELECT CODES

Q-Bit Code (Q09 through Q04)	Selected Rate (Bits per Second)
100000	50.0
100001	75.0
100010	110.0
100011	134.5
100100	150.0
100101	300.0
100110	600.0
100111	1,200.0
101000	1,800.0
101001	2,000.0
101010	2,400.0
101011	3,600.0
101100	4,800.0
101101	7,200.0
101110	9,600.0
101111	19,200.0

CHARACTER PARITY

Each port may be software-programmed for one of three parity modes: odd, even, or none. Parity is based on the number of bits in the data character. The receiver automatically checks for the correct parity. If one or more character parity errors are detected, the channel parity error (CPE) bit is set in the terminate status word following a normal terminate. The transmitter appends the parity bit to the data character prior to shifting the character out to the communication line.



CHARACTER LENGTH

Each port may be software-programmed for one of four data character lengths. Character lengths are exclusive of the parity bit and/or stop bit. Data characters may be five, six, seven, or eight bits in length. Unused bits appear as zeros in the high-order bit positions of an eight-bit character when the character length is five, six, or seven bits. Thus, one 16-bit processor word contains a maximum of two data characters regardless of length.

STOP BITS

Each port may be software-programmed for one of three stop-bit intervals. These stop bit intervals, in terms of bit times (at the programmed baud rate) are 1.0, 1.5, or 2.0. The stop-bit times are the minimum time intervals permitted between data characters. There is no maximum interval regardless of the stop interval selected. In operation, the transmitter automatically delays for the appropriate stop-bit interval before transmitting the next character. If the next character is not available to the transmitter, the stop-bit interval is simply continued until the character is loaded into the transmitter. The receiver detects the beginning of the stop element following the receipt of the correct number of data and parity bits. The actual stop-bit time is computed as follows:

$$\text{STOP BIT TIME} = \text{STOP BIT FACTOR} \times \frac{1}{\text{BAUD RATE}}$$

NORMAL MODE ENABLE/DISABLE

Each communication line transmitter or receiver of any BCLA port may be enabled or disabled by software. A disabled transmitter maintains a constant mark state on the transmit data (TD) line. A disabled receiver does not request service from the BCLA micro processor section regardless of the occurrence of state changes on the receive data (RD) lines. The channel should be disabled when not in service or when removing or connecting external communication line cables.

DATA LOOP-BACK TEST MODE

Each channel of the BCLA may be individually software-programmed to operate in an internal loop-back mode to verify a basic level of functional capability. In this mode, the receiver input from the communication line receiver is ignored; and the transmitter output to the line driver is disabled. The transmitter output is gated to the data input path to form a closed loop data path. The universal synchronous receiver/transmitter (USRT)

clear-to-send (CTS) input is held low, independent of the external CTS signal. Software requirements are the same as for normal, full-duplex operation. Termination of the buffer operation occurs as a result of EOT recognition, exhausting buffer length or error conditions. The mode is terminated by a master clear or normal mode command.

ECHO TEST MODE

Each port may be individually software-programmed to operate in an echo test mode. In this mode, data characters assembled by the port receivers are loaded into the port transmitter and returned to the sending terminal. The data service requests from the receiver are passed through the priority-resolving circuit. The transmitter control recognizes the echo test mode and waits for data from the receiver. The BCLA micro processor loads the transmitter with the just-received data characters. Any error conditions are ignored. If a character is received with bad parity, it is retransmitted as is but with a new and possibly different parity bit added. No data exchange with the processor memory takes place, nor are I/O buffers utilized. The mode is initiated by an A/Q write function and must be terminated by changing the port mode test bits and reissuing the A/Q write function.

ECHO-PLEX MODE

Any port may be software-programmed to cause retransmission of a received character, transparent of the processor software. In this mode, the BCLA receives data from the communication line and stores it in the processor memory buffer. In addition, each received character is echoed, via the tranmsmitter of the same port, to the sending terminal. Buffer terminations occur as in the normal mode. Setting and clearing of the echo-plex mode may be done at any time using the A/Q write function.

CR/LF PREFIX MODE

Any transmit channel may be software programmed to transmit an ASCII carriage return (CR) and line feed (LF) immediately following the A/Q write function of a transmit buffer length greater than zero. Following transmission of the CR/LF, the transmitter begins a normal buffer output operation. This mode terminates when the buffer terminates.

INSERT LF MODE

Any transmit channel may be software-programmed to transmit an ASCII line feed immediately following all ASCII carriage return characters detected in the output buffer. This mode terminates when the buffer terminates.

BLOCK MOVE OPERATION

Any port with an idle transmitter may be software-programmed to perform a processor memory-to-memory block move of up to 65,535 eight-bit bytes. The transmitter may be functioned simultaneously with a block move but only in the sequence of block move, then transmit. When the block move and transmit mode is programmed, the transmit begins as soon as the first word is moved in the processor memory.

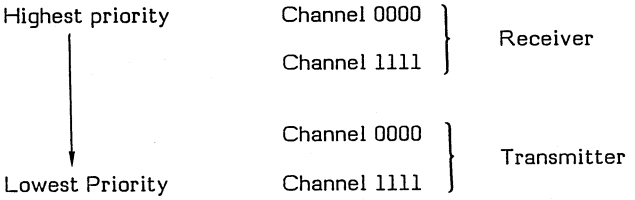
PROCESSOR-TO-BCLA INTERFACE

The transfer of control and data information between the CYBER 18 processor and the BCLA uses both the DMA and the processor A-register/Q-register (A/Q) buffered transfer modes of the processor.

SERVICE PRIORITY

Requests for service from the micro processor section of the BCLA are handled on a priority basis. When a receiver raises a request for service, the request is input to a priority-resolving circuit. This circuit generates the four-bit channel number, sets an internal condition flag to on, and inhibits further service requests until the current request is serviced.

Following the servicing of all receiver requests, the micro processor polls the transmitters. After the servicing of any one transmitter, a receiver may assume priority regardless of whether other transmitters require service. If two or more transmitters or receivers raise requests simultaneously, only one is recognized by the micro processor, based on the following scheme:



This priority scheme is applicable regardless of whether the system is configured with the expansion PWA (10 channels) or with the primary PWA (six channels) only. The maximum byte transfer rate for any combination or number of receivers and transmitters is 30,720 bytes per second.

DMA I/O INTERFACE

The DMA I/O mode is used to transfer data between buffers in the processor macro memory and the communication channels. The common controller portion of the BCLA (figure 1-2) includes the hardware for the DMA interface.

The BCLA receives buffer control information from software via the A/Q function format; it maintains up to 16 block move, 16 receive, and 16 transmit buffer control parameters at any one time. The basic elements of the buffer controls from software are first word address (FWA) and buffer length, in bytes.

The BCLA maintains five basic controls: next word address, current byte count, terminate mode (EOT or buffer length), test or normal mode, and buffer active/buffer complete.

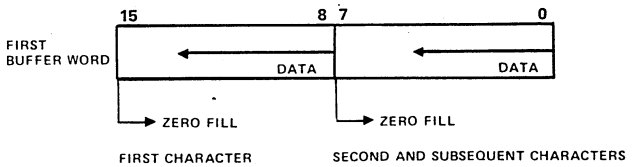
Next word address is used to access a 16-bit processor macro memory word. When a channel is transmitting, the BCLA reads one word out of memory for every two bytes transmitted. When receiving, the BCLA writes one word to memory for every two bytes received. If a receive buffer terminate results in a half-word, the BCLA zero-fills the remainder of the word.

The current byte count for each buffer is compared to the buffer length each time a byte is transferred to or from the BCLA. This comparison occurs in the EOT mode and buffer length mode. When the buffer equals the current byte count, the BCLA terminates the buffer activity.

Receive/Transmit Buffer Location

These two fields indicate the start location of the I/O buffers in macro memory. There are no restrictions on I/O buffer locations. However, BCLA overhead time is increased if address incrementation during DMA data transfers causes an overflow to bit 17.

The BCLA reads or writes a 16-bit word when accessing memory. If the channel is programmed for five-, six-, or seven-bit characters, the low-order bits are considered valid data. The BCLA sets the unused (high-order) bits of the eight-bit character field to zero, as shown below:



Receive/Transmit Buffer Length

The maximum buffer length in eight-bit bytes is 65,535 bytes. A buffer length of zero results in an immediate program interrupt with termination status available. No data transfers occur. If the buffer length (in characters) is not modulo two, the final received character is stored left-justified in the final buffer word. The eight least significant bits (LSBs) of the word are set to zero.

Block Move Buffers

Block move buffers start on word boundaries. The block move length is in bytes (for compatibility with the transmit buffer length). However, the move is by 16-bit words. If the length (in bytes) is odd, the value is rounded up by one byte, and one-half the resulting number of words is moved as a block. A block move of length zero has no meaning and results in a reject if issued by software. Any of the 16 ports may be used for a block move, independent of the installation of an expansion BCLA.

A/Q INPUT/OUTPUT INTERFACE

The A/Q input/output mode is used for control and status operations. No data is transferred to or from the line or processor via the A/Q mode. There are two A/Q register formats. One format, referred to as the write or function format, is used for control outputs to the BCLA. The second format, referred to as the read or status format, is used for reporting the status of the BCLA.

Function Format

The function or write format, figure 2-2, is used to transfer control information required by the BCLA to perform transmit, receive, block move, or test operations.

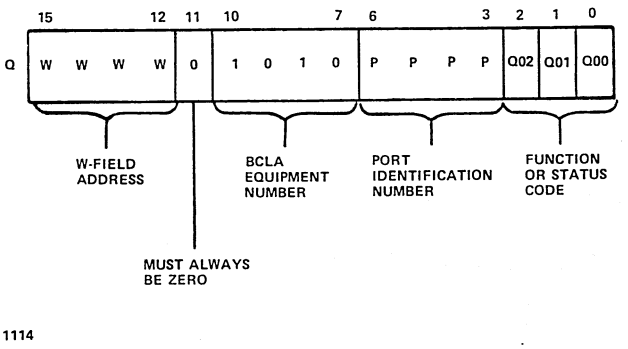


Figure 2-2. Q Register Function and Status Format

Bits Q02, Q01, and Q00 define the eight functions listed in table 2-4. The contents of the A register are interpreted by the BCLA based on these bits.

TABLE 2-4. CONTROL BIT ASSIGNMENTS

Q02	Q01	Q00	Control Function
0	0	0	Port mode set-up
0	0	1	Receive buffer transfer
0	1	0	Transmit buffer transfer
0	1	1	Block move source
1	0	0	Optional port control
1	0	1	Receive buffer length
1	1	0	Transmit buffer length
1	1	1	Block move length

Bits Q06 through Q03 identify the specific port (channel) on the BCLA and may have any value from 0000 through 1111 (decimal 0 through 15).

Bits Q10 through Q07 identify the equipment number assigned to the BCLA, which is always 1010. This code is established by the jumper plugs at primary PWA location U64 (figure 1-2).

Bit Q11 must always be zero.

Bits Q15 through Q12 form the W-field address for the specific BCLA and may have any value from 0001 through 1111; they may not have a value of zero. This address is established by the DIP switch at primary PWA location U126 (figure 1-2) and is defined in table 2-1.

Port Mode Setup

When bits Q02, Q01, and Q00 are equal to 000, the operating mode of a port is set. The operating mode is required only once per port following power-on or master reset. This command may be issued at any time to change

a port mode set-up. The port should be inactive when setting the mode. Figure 2-3 identifies the A-register contents used for setting the port mode. The modes are defined in the programmable operating modes subsection earlier in this section.

A normal port mode set-up resets the port in the following manner:

- All test modes are cleared.
- The receiver and transmitter are disabled.
- Data terminal ready (DTR) is off.
- Request to send (RTS) is off.
- The port is ready for the next transmit, receive, or test operation.

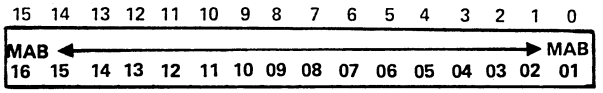
The loop-back test mode requires received and transmit buffer set-ups. Loop-back operation is initiated using the same procedure as a normal (full-duplex) data transfer after the port mode has been set to loop-back test. The echo-test mode is effective immediately following the mode set-up A/Q write command.

Master clear resets all ports of the BCLA; it requires PPPP of the Q register to equal 0000 and causes the BCLA to go busy for 40 microseconds. After a master clear, the state of the BCLA is as follows:

- All interrupts cleared
- Data transfer rate of 9,600 bits per second selected
- Seven bits per character format
- One stop bit
- Even parity
- RTS, DTR, and TD in a marking condition
- Modem interrupts masked until a port mode function command is issued. Data set ready (DSR) and data carrier detect (DCD) are always available as status.

Receive Buffer Transfer

With Q02, Q01, and Q00 equal to 001, the receive buffer first word address (FWA) bits 1 through 16 are transferred to the port designated by PPPP of the Q register (figure 2-2). The A-register format is as follows:



Where MAB is the memory address bit. This function is always required for a receive buffer operation. Figure 2-4 illustrates the receive initiation sequence.

Transmit Buffer Transfer

Function code 010 transfers the transmit buffer FWA bits 1 through 16 to the port designated by PPPP of the Q register (figure 2-2). The A-register format is the same as for receive buffer transfer. This function is always required for a transmit buffer operation. Figure 2-5 illustrates initiation sequences.

Block Move Source

Function code 011 transfers the block move source FWA bits 1 through 16 to the port designated by PPPP of the Q register. The A-register format is the same as for a

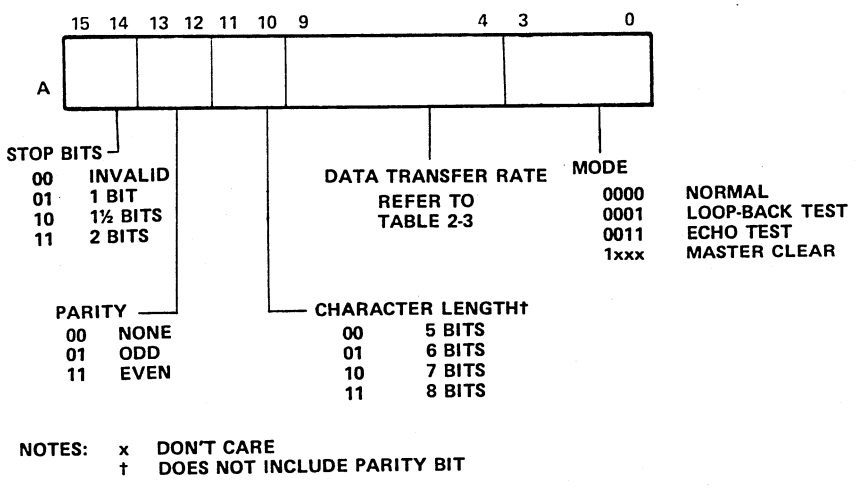
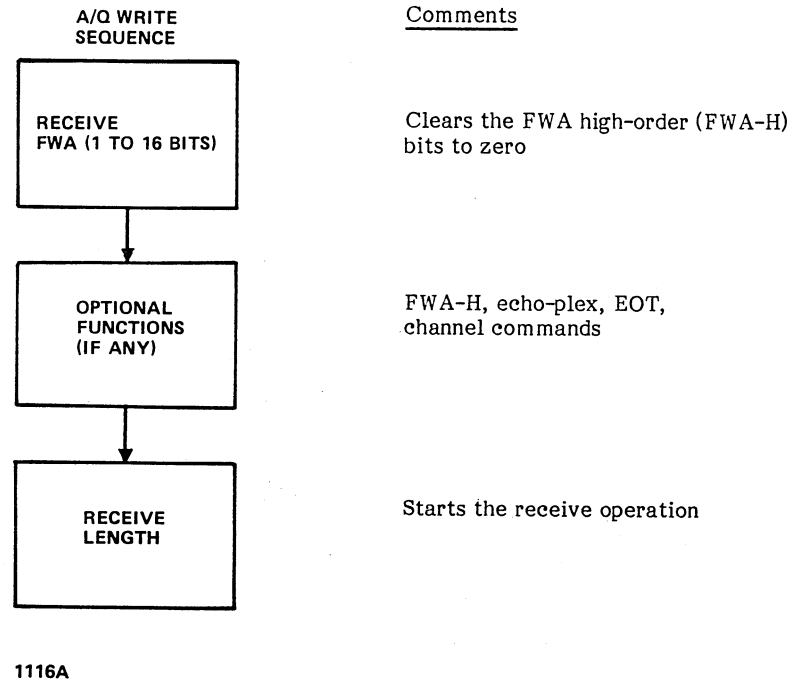


Figure 2-3. A Register Port Mode Bit Configuration



Figue 2-4. Receive Initiation

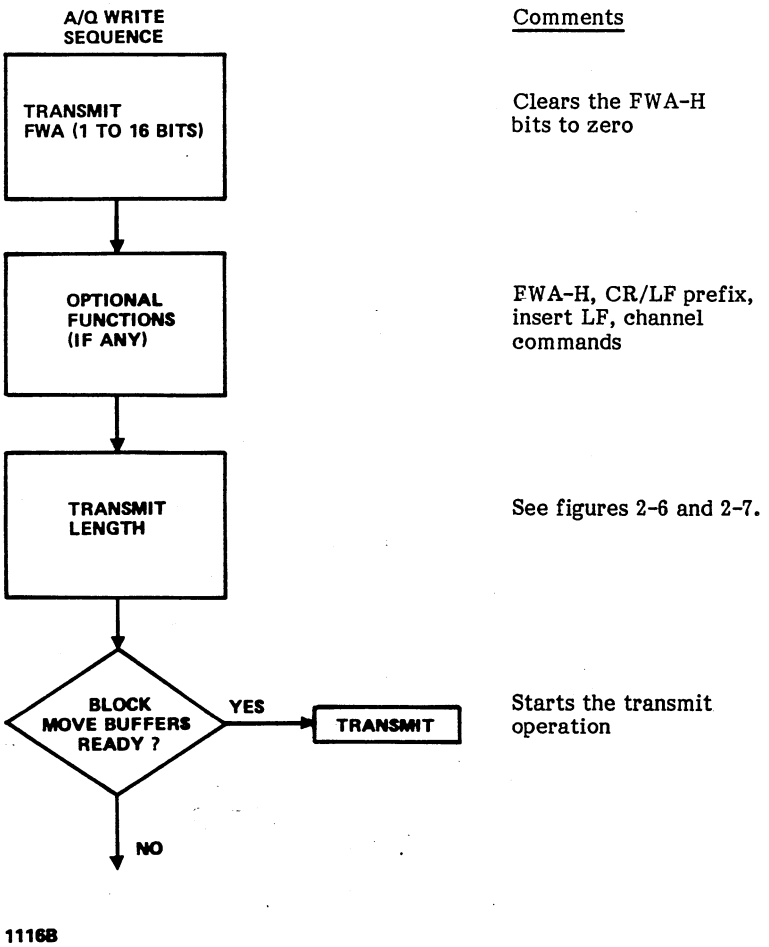


Figure 2-5. Transmit Initiation

receive buffer transfer. This function is always required for a block move operation. Figures 2-6 and 2-7 illustrate the block move and block/transmit initiation sequences.

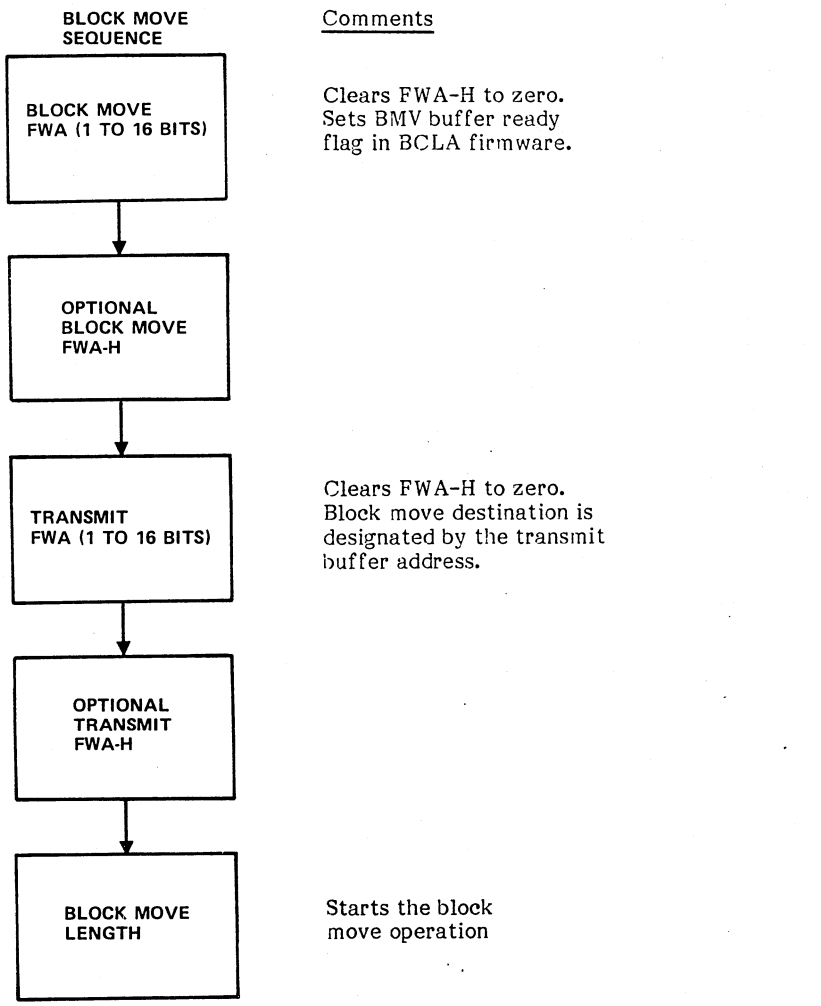
Optional Port Controls

A function code of 100 indicates that the A-register contents consist of either a subfunction code or a subfunction code and port/buffer control information. The function is deemed optional since it need not be issued each time a buffer is initiated. The contents of the A register are decoded into nine different optional functions that may be programmed into the operation of any port. Five of these function formats use the full 16 bits of the A register (A upper and A lower). The remaining four formats use only the lower eight bits of the A register. All unused bits are filled with zeros. Table 2-5 summarizes nine optional port controls.

Carriage Return/Line Feed - When this function (00_{16}) is included with a transmit buffer set-up, the BCLA transmits an ASCII carriage return followed by a line feed command

TABLE 2-5. OPTIONAL FUNCTION CODES

Function	Hexidecimal Code	A Code
CR/LF prefix	00	0 0 0 0 0 0 0 0
Insert LF	02	0 0 0 0 0 0 1 0
Echo-plex off	04	0 0 0 0 0 1 0 0
Echo-plex on	06	0 0 0 0 0 1 1 0
Post command	01	0 0 0 0 0 0 0 1
Receive FWA-H	03	0 0 0 0 0 0 1 1
Transmit FWA-H	05	0 0 0 0 0 1 0 1
Block move FWA-H	07	0 0 0 0 0 1 1 1
EOT character	Fx	1 1 1 1 n n n n



NOTE: PROGRAM INTERRUPT IS SET TO ON WHEN THE BLOCK MOVE IS COMPLETE.

1116C

Figure 2-6. Block Move Initiation

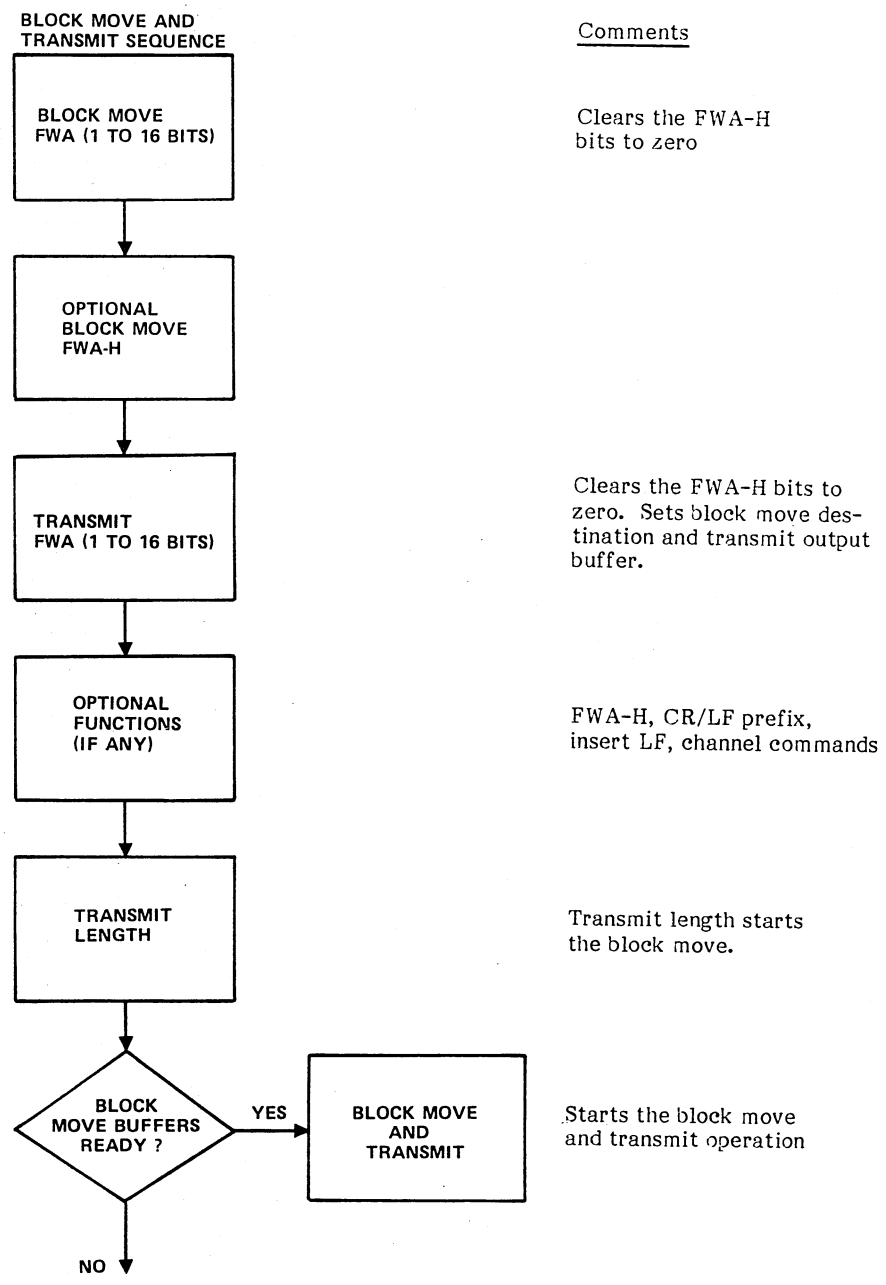


Figure 2-7. Block Move and Transmit Initiation

(hexadecimal 0D0A) prior to initiating the transmission of buffer data. This function is terminated when the buffer terminates. The two prefix bytes are not reflected in the total transmitted byte count status.

Insert Line Feed - When this function (02_{16}) is included with a transmit buffer set-up, the BCLA transmits an ASCII line feed command (hexadecimal 0A) following the detection of any ASCII carriage return character in the transmit buffer. This function is terminated when the buffer terminates. The inserted bytes are not reflected in the total transmitted byte count status.

Echo-Plex Off - This function (04_{16}) may be issued to the BCLA at any time for any port not in a test mode. It causes the port to cease echo-plex operation but continue normal receive operation. A transmitter used for echoing data is dedicated to this function and transmits only data received from the port receiver. The BCLA controls the transmitter whenever the receive operation of a port is programmed for echo-plex or the port mode is echo test.

Echo-Plex On - This function (06_{16}) may be issued to the BCLA at any time for any port not in a test mode. In echo-plex mode, each character received from the communication line without buffer terminating errors is retransmitted from the port where it was received. The character is also handled as a normal received character and stored in the processor buffer. Buffer termination is not changed from normal operation.

Port Command - The port command function (01_{16}) is included in the optional group, although it is normally required at least once per port following a master reset. The function causes the literal in A upper to be loaded directly into the communication port output control register. Figure 2-8 illustrates the port command function bits.

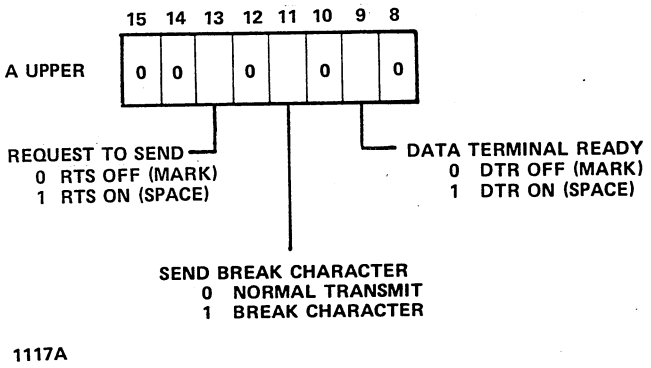
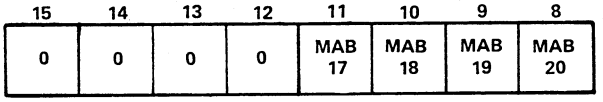


Figure 2-8. Port Command Function Bits

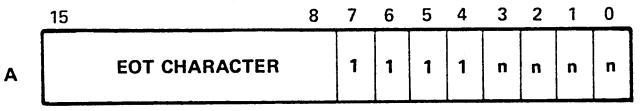
First Word Address - The FWA functions (03_{16}, 05_{16}, 07_{16}) are used to send to the port the high-order bits of the receive, transmit, and block move buffer first word addresses.

These functions are required only if the DMA address exceeds 16 significant bits. The format for A upper is as follows:



The BCLA sets these four high-order address bits of the DMA buffers to zero upon receipt of the 16-bit FWA. Therefore this function is required after an FWA command for addresses greater than 16 bits.

End-of-Text Characters - The end-of-text (EOT) function (Fx_{16}) sets or clears the EOT mode and sends an EOT character to the designated port. The A-register format for this function is as follows:



This function defines the literal in A upper as an EOT character. Up to 10 EOT characters per receive channel may be sent to BCLA. The BCLA stores these characters in a 10-entry table. nnnn determines the position in the table and the length of the table as follows:

- There must always be an EOT with nnnn equal to 0001.
- nnnn numbers must be contiguous (no gaps).
- The highest numbered EOT must be sent last; conversely, the nnnn sent last is assumed by the BCLA firmware to be the length of the list (0001 = 1, 1010 = 10).
- When nnnn equals 0000, there are no EOTs; this condition may be used by the software to switch off the EOT mode while the BCLA retains the list(s) previously sent. In this case, A upper must be hexadecimal 00 when nnnn equals 0000. To re-enable the EOT mode, the software reissues this function with nnnn and EOT equal to the last EOT sent when the list was initially established or any new length designated.

The BCLA scans the EOT characters in the tables in reverse order to their ranking. To minimize BCLA overhead, the EOT most frequently expected should be assigned the highest nnnn number. The remaining EOTs should be ranked accordingly.

Receive Buffer Length

Function code 101 transfers the receive buffer lengths (in bytes) to the port designated by PPPP of the Q register (figure 2-2) and initiates channel operation. The 16 bits of

the A register specify the buffer length. Hexadecimal 0000 equals zero bytes. Hexadecimal FFFF equals 65,535 bytes, the maximum buffer length. This function is always required for a receive operation.

Transmit Buffer Length

Function code 110 transfers the transmit buffer length (in bytes) to the port designated by PPPP of the Q register (figure 2-2). It also initiates channel operation and a block move, if a block move source buffer FWA has been established. The 16 bits of the A register specify the buffer length with the same limitations as for the receive buffer length. This function is always required for transmit or transmit/block move operations.

Block Move Length

Function code 111 transfers the block move buffer length (in bytes) to the port designated by PPPP of the Q register (figure 2-2) and initiates the block move only operation. The 16 bits in the A register specify the buffer length in bytes, but move is by words. If the length is odd, the byte length +1 is moved. This function is always required for a block move only operation. The block move destination buffer is the transmit buffer.

Status Format

The status or read format, figure 2-2, is used to read status from the BCLA. A status read is performed in response to an interrupt from the BCLA. The software uses this information to determine which BCLA and/or channel caused the interrupt. Bits Q02, Q01, and Q00 specify the type of status to be read from the BCLA; these bits are defined in table 2-6. Bits Q15 through Q03 provide the same information during a status format as previously described for a function format.

TABLE 2-6. STATUS BIT ASSIGNMENTS

Q02	Q01	Q00	Assignment
0	0	0	Normal interrupt status (unique BCLA)
0	0	1	Port receive operation byte count
0	1	0	Port transmit operation byte count
0	1	1	Port extended status
1	0	0	Break/clear-to-send (CTS) status
1	0	1	A/Q echo check (diagnostic)
1	1	0	Not used
1	1	1	Special interrupt status (shared interrupts

Normal Interrupt Status

A status code of 000 in bits Q02, Q01, and Q00 defines a normal interrupt status read code used following an interrupt and/or the special status read. Bits Q15 through Q12 (W field) identify a BCLA that has been determined to have interrupt status pending. Bits Q06 through Q03 (port number) are not applicable to this status code and are ignored by the BCLA. Following this status read, the A register has the format shown in figure 2-9. A binary 1 bit in a field indicates the presence of a condition unless otherwise specified in the following descriptions. PPPP is the identification number of the port that caused an interrupt to be set on.

Interrupt Types - Normal status interrupts provide the following types of status to the A register:

T - The interrupt was caused by a transmit operation termination resulting from a buffer length exhausted condition. This status type may be set on simultaneously with status type R below.

R - The interrupt was caused by a receive operation termination. Software should check for error bits also when this status is reported. This status type may be set on simultaneously with status type T above.

EOT - This bit set to 1 indicates that a receive operation terminated as a result of an EOT comparison. The EOT character is stored last in the receive buffer. If this bit is 0, the receive operation terminated as a result of a buffer length exhausted condition or a channel error.

M - This interrupt is caused by the completion of a block move operation.

MDM - This interrupt results from a change of state of modem lines DCD or DSR.

NIP - With this bit set, no interrupts are pending.

Various conditions cause the BCLA to set an interrupt on. The conditions are related to a specific port and cause a status word to be stored in a BCLA register associated with that port. There may be up to 16 status words stored at any one time. Upon receipt of a status read, the BCLA transfers one of the status words to the A register. The status read is reissued repeatedly to obtain a complete listing of pending status words. When there is no further status to report, the BCLA sets the NIP bit and turns off the interrupt. For any interrupt, the minimum number of status reads is two.

Channel Errors - Three types of channel errors may be reported as status:

BFE - This bit indicates that a break or framing error occurred during a receive operation. The BCLA terminates the receive operation immediately, unless the no-stop-on-error jumper is in, and sets the program interrupt on. R is also set to 1.

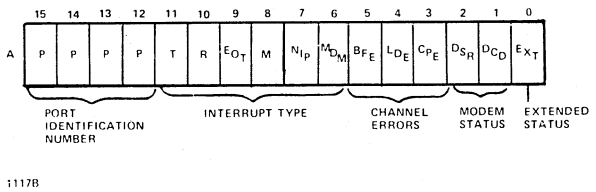


Figure 2-9. A-Register Normal Status Format

LDE - This bit indicates that a lost data error has occurred during a receive operation. The BCLA terminates the receive operation immediately unless the no-stop-on-error jumper is in, sets the program interrupt on, and sets R to 1.

CPE - This bit indicates that a channel parity error has occurred during a receive operation. The BCLA continues to transfer data until a normal terminate occurs. Following the normal terminate, the BCLA sets bit A03 to 1 to indicate the error, sets the program interrupt on, and sets R to 1.

If the no-stop-on-error jumper is installed (figure 1-2, location U64), BFE or LDE does not terminate the buffer. Only the normal (EOT or buffer length exhausted) terminate effective. The BFE and/or LDE bits appear in the termination word status.

Modem Status - Two types of modem status may be reported as status:

DSR - This bit indicates the status of the modem data set ready line:

0 = Off (mark) 1 = On (space)

DCD - This bit indicates the status of the modem data carrier detect line:

0 = Off (mark) 1 = On (space)

Extended Status - The extended status (EXT) bit indicates that an error has occurred while accessing the processor memory during a DMA cycle. The extended status word is available via an extended status read.

Receive Byte Count

A status read code with Q02, Q01, and Q00 equal to 001 is not directly related to interrupt conditions and may be issued at any time. The code reads the BCLA register file locations that contain the number of bytes transferred on the last receive operation. The port is specified by PPPP of Q. This status is useful following an EOT or error termination. After the status read, the 16 bits of the A register specify the number of bytes last stored in the receive buffer.

Transmit Byte Count

A status read code with Q02, Q01, and Q00 equal to 010 is not directly related to interrupt conditions and may be issued at any time. This code reads the BCLA register file locations that contain the number of bytes transferred on the last transmit operation. The port is specified by PPPP of Q. This status is useful following an error termination. After the status read, the 16 bits of the A register specify the number of bytes last transmitted from the transmit buffer.

Extended Status Read

This status read code (Q02, Q01 and Q00 equal to 011) is used to read the extended status word (ESW) from a BCLA port. The port number is specified by PPPP of Q. After this status read, the A register has the format shown in figure 2-10 and defined by the following terms:

PORT ID - PPPP (0000 through 1111) identifies the port that initiated the DMA cycle.

MAE - Memory address error:

T - MAE occurred during a transmit operation.

R - MAE occurred during a receiver operation.

MR - MAE occurred during a block move read.

MW - MAE occurred during a block move write.

MPE - Memory parity error:

T - MPE occurred during a transmit operation.

R - MPE occurred during a receive operation.

MR - MPE occurred during a block move read.

MW - MPE occurred during a block move write.

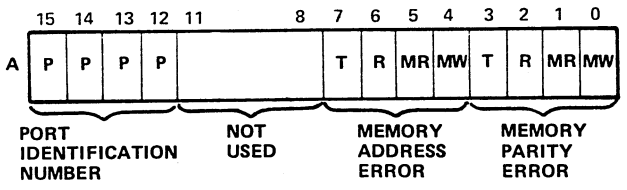


Figure 2-10. A-Register Extended Status Format

Memory errors do not affect buffer operations or move operatons. Following a normal terminate, the occurrence of an MPE or MAE is reflected in the extended status bit of the normal interrupt status word.

Break and CTS Status

A status read code with Q02, Q01, and Q00 equal to 100 reads the communcation interface device status register (universal synchronous/asynchronous transmitter/receiver, USART, status). The port is specified as PPPP of Q. After the read, the A-register contents are as shown in figure 2-11.

Clear-to-send status is provided for diagnostic use only and is not considered valid until a minimum of 12 microseconds after setting the port to the loop-back test mode. Diagnostic software must ensure the delay. The port is set to the loop-back test mode using the port mode set-up A/Q write function. Actual loop-back operation is not required and does not occur unless a buffer set-up sequence is completed.

The break condition is defined as the receipt of an all-zero word of programmed length, including the start bit, data bits, parity bit, and one stop bit. The start and end of break are determined as shown in figure 2-12.

A/Q Echo Check

A status code with Q02, Q01, and Q00 equal to 101 provides a diagnostic echo check of the BCLA. After the read, the contents of the A register are expected to be hexadecimal FF00. Correct receipt of the pattern assures that the BCLA is operating and that the W-field and equipment device codes are properly selected.

Special Interrupt Status

A status code of 111 in bits Q02, Q01, and Q00 defines a special interrupt status and must precede the normal status interrupt if multiple BCLAs are sharing the same processor interrupt.

Bits Q15 through Q12 identify the master primary BCLA. W=1111 has been assigned for the special interrupt status. The W field is a system convention only. If any other W field is used, that BCLA transfers the state of the external interrupt pins to the A register. Therefore, the installation interrupt wiring configuration and software drivers must be coordinated. The special interrupt status is not required if the processor interrupt line is unique to one BCLA. Bits Q06 through Q03 are not applicable to the special interrupt status and are ignored by the BCLA.

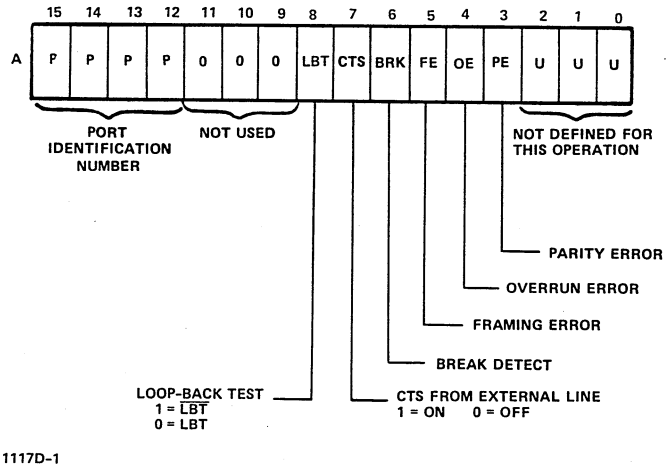


Figure 2-11. Communication Interface Status Format

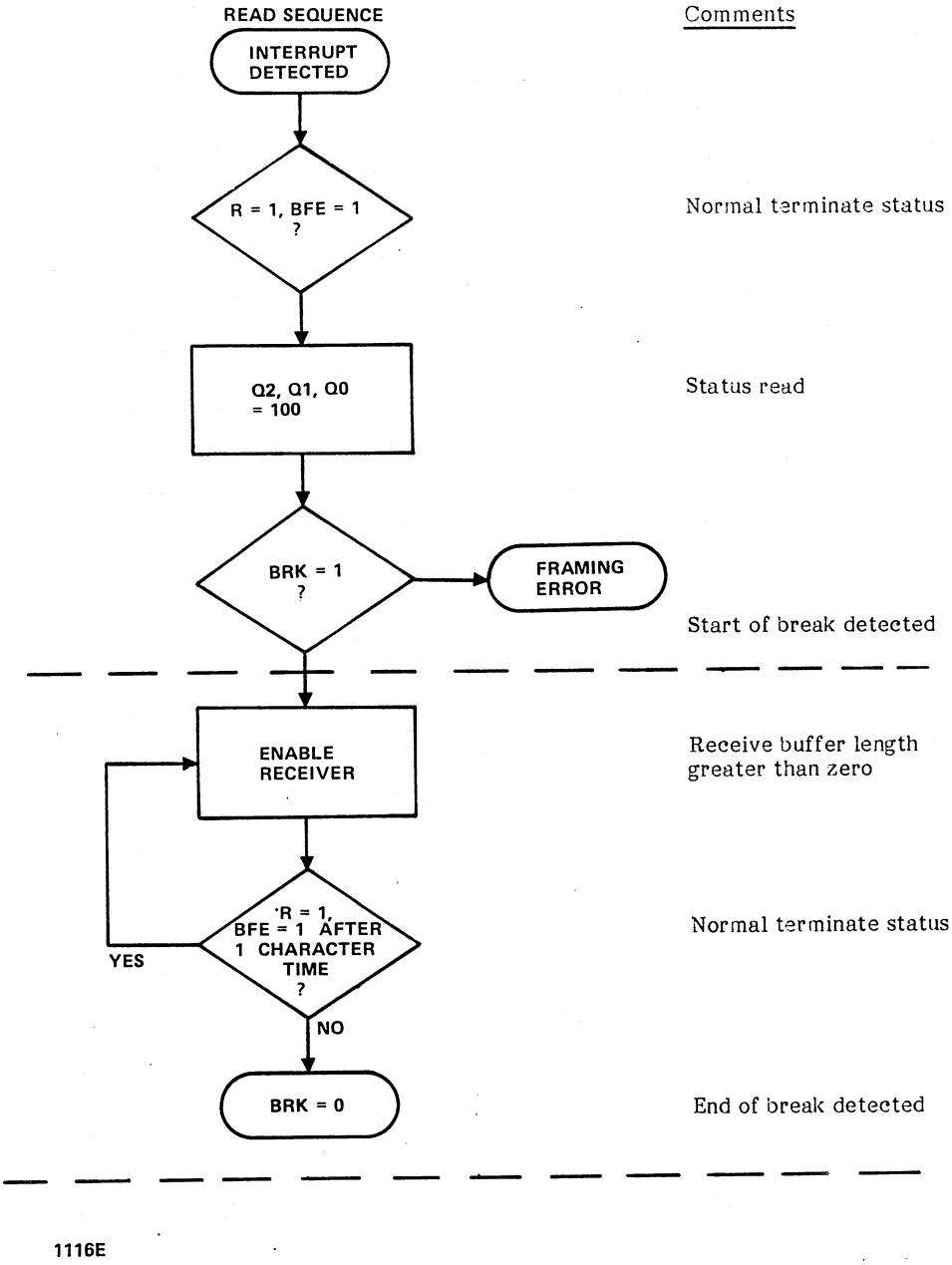


Figure 2-12. Break Distribution and Termination

After a special interrupt status read, the A register has the format shown in figure 2-13. The position in the field need not correspond to the number in the BCLA W field. The software must maintain the loop-up table to derive the BCLA number. After identifying the BCLA with the active interrupt, the software must perform a normal interrupt status read of each active BCLA to determine the channel number and status interrupt conditions.

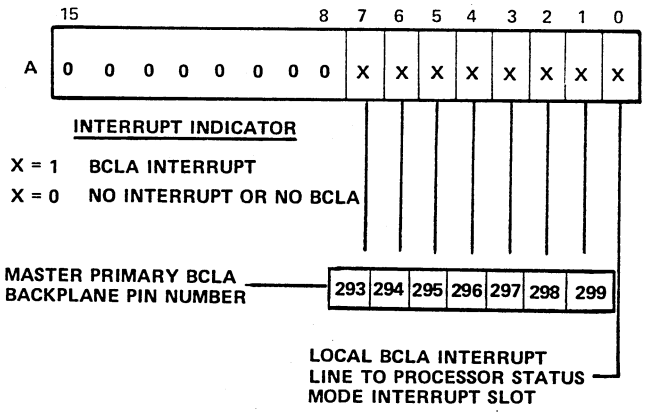


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Figure 2-13. A-Register Special Status Format

BCLA-TO-COMMUNICATION-LINE INTERFACE

Each communication line (channel) terminated at the BCLA consists of the signals listed in table 2-7. The signals are identified by the BCLA, RS232-C, and CCITT V.24 mnemonics. The data signal rate select (SR) signal is implemented on the processor backplane adapters (figure 1-4) and does not appear on the BCLA printed wiring assembly. This signal is always in the on (space) state at the I/O connector panel.

TABLE 2-7. COMMUNICATION LINE SIGNALS

BCLA Mnemonic	Function	RS-232-C Name	CCITT V.24 Name
FG	Frame ground	AA	101
TD	Transmitted data	BA	103
RD	Received data	BB	104
RTS	Request to send	CA	105
CTS	Clear to send	CB	106
DSR	Data set ready	CC	107
SG	Signal ground	AB	102
DCD	Data carrier detect	CF	109
DTR	Data terminal ready	CD	108.2
SR	Data signal rate select	CI	112

Following a master reset power-on reset to the BCLA, the active signal lines controlled by the BCLA assume the state shown below. Control of these signals is via software.

Signal	State
TD	Mark (stop element)
RTS	Mark (off)
DTR	Mark (off)

The TD signal follows the bit pattern of the data in the transmit buffer based on the following relationship:

Software Buffer Data Bit	Reference	Communication Line
Binary 1 or high	1	Mark
Binary 0 or low	0	Space

TD is forced to a continuous space condition when software sets the send break character bit to a binary 1 (high) in the control table. TD remains in the mark state, independent of software control, if the incoming CTS signal is in the mark (off) state. TD remains in the mark state following a transmit function.

RTS and DTR relate to bits set by software as follows:

A-Register Control Bit	Reference	Communication Line
Binary 1 or high	1	Space (on)
Binary 0 or low	0	Mark (off)

RD, received from remote terminals or modems, produces a bit pattern in the receive buffer on the following relationship:

Software Data Buffer Bits	Reference	Communication Line
Binary 1 or high	1	Mark
Binary 0 or low	0	Space

Based on the software-selectable data transfer rate, stop-bit length, and data character length, the BCLA assembles valid data characters from the RD line. If the line changes from the mark state to the space state and remains in the space state in excess of one character time, the BCLA detects a framing error. Upon detection of a framing error, the BCLA sets up a status word for transfer to the A register and sets the program interrupt on.

CTS in the mark (off) state inhibits operation of the channel transmit function. No data is transmitted from the buffer unless CTS is on. A software time-out may be used to detect a failure to transmit.

CAUTION

CTS RESTRICTION: The BCLA may produce data transmission errors when transmitting to a device that uses CTS to halt that transmission unexpectedly (for example, as a restraint function). CTS cannot be depended upon to halt a transmission in progress with the expectation that transmission can be resumed without error.

If CTS is dropped while a character is being transmitted, that character is completed and the transmission halted. When CTS is turned on again, transmission resumes; however, the previously interrupted character may be retransmitted.

To avoid this problem, the communications subsystem should drop CTS between, rather than during, data buffer outputs. CTS operation meets all of the RS232 requirements for the control of half-duplex modems.

DSR and DCD are monitored on a polling basis by the BCLA. Any change of state (on to off or off to on) of either signal or both signals sets the BCLA program interrupt on. The state of the two signals is stored in the termination status word.

DCD and DSR in conjunction with DTR permit connect and disconnect capability with phone lines on dial-in calls. The auto-answer capability must be in the modem. The software must hold DTR on. The incoming call to the modem causes the modem to go off-hook, and the modem sets the DSR on. Upon recognition of DSR, software starts a timer; and the modem waits for a carrier signal from the phone line. When the carrier is detected, the modem sets DCD on. The software assumes a viable data channel to a remote terminal upon recognition of DCD. If the modem is dialed erroneously, DCD is not asserted within the software timer interval; and software causes the modem to go on-hook to await a valid call. In either a wrong number or a valid call situation, software may cause the modem to go on-hook by setting DTR off, which causes the modem to drop DSR. DTR is then reset by the software to await another call. If DCD is lost during a transmission, DTR hangs up and re-enables the modem. After a master clear, either internal or external, the DSR and DCD state change interrupts are masked. A port mode A/Q write to any port clears the mask for all ports. During the time that the DSR and DCD interrupts are masked, their current state is available in the termination status word. Access to this status word may be forced by causing a termination status (for example, transmit length equal to zero, receive length equal to zero, or a block move).

INSTALLATION 3

For detailed installation procedures of the buffered communication line adapter, refer to the CYBER 18 computer system installation manual listed in the preface.

THEORY OF OPERATION 4

This section contains external and internal interface diagrams, tables, and logic functional descriptions. The diagrams depict the source and termination of read, write, and control signals for the common controller and the communication interface. The tables list and define the signal application. The text describes the block diagrams that represent the operaton of the logic diagrams. The block diagrams contain blocks that represent functional groups of logic. Numbers appearing in the upper right corner of each block indicate the logic diagram sheet number that contains the functional logic group.

EXTERNAL INTERFACE

Figures 5-1 and 5-2 indicate the source and termination points of data and control signals applicable to the primary and expansion BCLA printed wiring assemblies, respectively. Table 4-1 tabulates the primary BCLA signals in alphabetical sequence and provides a definition and description of each mnemonic appearing in figures 5-1 and 5-2. Table 4-2 lists, defines, and describes the signals applicable to the expansion BCLA.

The signal names in the logic diagrams use diagonal (/) and bar (—) symbols to indicate the active (low) condition of the signal. The diagonal is applied to the mnemonic of external interface signals; the bar is applied to the mnemonic of internal signals. (For example, ARD0/ through ADR11/, CHARINPUT/, and RD01/ through RD16/ are external active signal notations; and BG0 through BG8, LDDMAH, and LOADFA are internal active signal notations.)

OVERALL FUNCTIONAL DESCRIPTION

The BCLA subsystem (figure 4-1) may include six or sixteen communication ports contained on one or two printed wiring assemblies (primary BCLA, six ports; expansion BCLA, ten ports). The primary BCLA PWA contains the logic of the common controller (firmware-controlled micro processor) and communication interface (control and data for six communication ports, 00-05). The expansion BCLA contains the communication interface for 10 additional communication ports (06-15). Each port consists of a transmit (write) channel and a receive (read) channel and may transfer data in half duplex (write or read separately) or full duplex (write and read simultaneously). Data (transmit and receive) is transferred between the BCLA and modem or terminal in serial format using RS232 voltage interface or 20 mA current loop/RS232 voltage interface adapters. Data is transferred between the communication ports and the common controller in parallel format over three-state bi-directional buses. Data is transferred between the BCLA and the CPU via the direct memory access (DMA). The CPU control (command and function) is transferred between BCLA and the CPU via A/Q lines (address, send data, and read data).

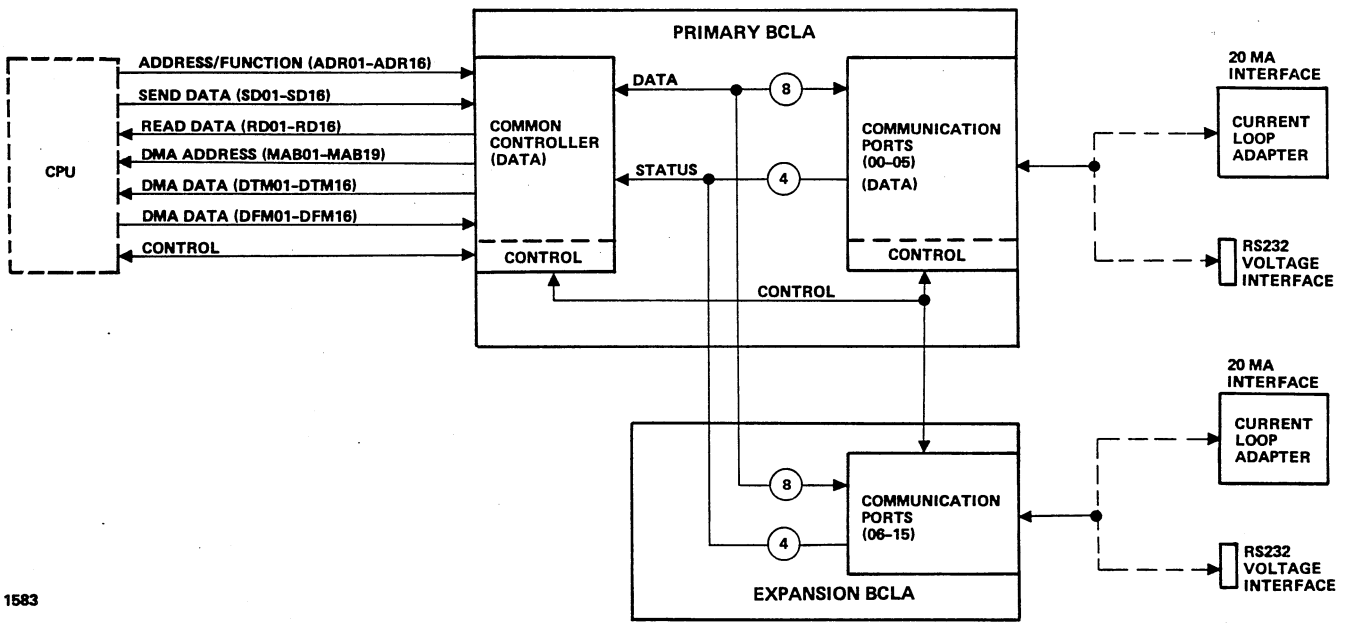


Figure 4-1. BCLA Block Diagram

TABLE 4-1. PRIMARY BCLA EXTERNAL SIGNALS

Term	Definition	Description
ADR01-ADR16	Address bits 01 through 16 (origin: Q register)	Address code to designate the function/status code, port identification, equiment, and active BCLA
CLK	Clock signal	12.0 MHz clock pulses for external timing applications
CTS00-CTS15	Clear to send, ports 00 through 15	This signal is received from the modem. It enables or inhibits the transmit channel of the associated port.
DCD00-DCD15	Data carrier detected, ports 00 through 15	This signal is received from the modem. It enables or inhibits the receive channel of the associated port.
DFM01-DFM16	Data from memory, bits 1 through 16	DMA data obtained from the processor main memory for/transmission to a terminal
DTM01-DTM16	Data to memory, bits 1 through 16	DMA data received from the terminal or buffer for/storage in the processor main memory
DMA-MAB01-DMA-MAB19	DMA memory address, bits 1 through 19	Designates the main memory location for storage or/retrieval of data
DMA-MAE	DMA memory address error	Designates that a memory address error occurred
DMA-MDS	DMA memory data strobe	Strobe data into the date from memory register
DMA-MPE	DMA memory parity error	Indicates that a memory parity error occurred
DMA-PF	DMA memory protect fault	Indicates that a protected memory area was designated but the protect requirements were not met
DMA-PROT	DMA protected	Indicates that the BCLA is requesting a protected DMA operating mode
DMA-WRITE	DMA write	Specifies direction of DMA data flow: BCLA processor = write active, processor to BCLA = write inactive
DMAx-INT	DMA internal	Most significant DMA address bit
DMAx-RA	DMA request accepted	Enables the DMA data transfer sequence
DSR00-DSR15	Data set ready, ports 00 through 15	Indicates to the associated port that modem is ready
DTR00-DTR15	Data terminal ready, ports 00 through 15	A query from the associated port to the modem to check status
MR	Master reset	Master reset from the processor. Causes the BCLA to go busy for 40 micro-seconds. Issued to change a port-mode setup.
PROGPROT	Program protected	Designates that the I/O instruction is protected
RD00-RD15	Receive data lines, ports 00 through 15	Serial data input to associated port receive channel
RD01-RD16	Read data, lines 01 through 16	Open collector lines for transfer of data to the processor A register

TABLE 4-1. PRIMARY BCLA EXTERNAL SIGNALS (Contd)

Term	Definition	Description
READ	Read select	Selects the status input to the processor A register
REJECT	Reject	Rejects the requested A/Q operation
REPLY	Reply	Replies to the requested A/Q operation
RPINT	Program interrupt	Designates that a BCLA channel requires A/Q service
RTS00-RTS15	REQUEST to send	Advises the modem that the associated port has data to transmit
SD01-SD16	Send Data, line 1 through 16	Direct function and data transfer lines to the processor A register
Slow DMA	Slow DMA	Indicates DMA data transfer employs slow rate
TCLK	Time clock Signal	6.0 MHz clock pulses for external timing application
TD00-TD15	Transmit data lines, ports 00 through 15	Serial data output from the associated port transmit channel
TEST	Test of BCLA controller	Enables test operation
WE0	W field equals zero	Q register command word BCLA select field (W). This signal must be high to initiate BCLA operation.
WRITE	Write	Enables the function word transfer from the processor A register
STOP THE CLOCK	Stop the Clock (Not for field use)	Input (low) required to stop the common controller and communication interface sync clocks when testing for reprogramming the BCLA PWA
EXT FREQ	External frequency input (Not for field use)	Used when testing or reprogramming the BCLA PWA

TABLE 4-2. EXPANSION BCLA EXTERNAL SIGNALS

Term	Definition	Description
ALU4-ALU7	Arithmetic logic unit output bits 4 through 7	Selects the baud rate output of the baud rate generators
BRGSTB	Baud rate generator strobe	Initiates the baud rate decoder selection of an associated baud rate generator strobe
C/D	Control/not data	Designates that the USART data bus content is either a control (C) or a data (D) character
CHIP ENABLE	Chip enable	Enables or inhibits the (USART) chip select decoders
CHRD	Character read	Enables the read operation of the USART
CHWR	Character write	Enables the write operation of the USART
DSR-DCD	Data set ready-data carrier detected	Enables the selection of the data set ready or data carrier detected status from the modem
MC	Master clear	Resets the BCLA registers
PE-PNR	Priority encoder or Port number register	Transfers the active receiver port number to the port number register
PNR1,2,4,8	Port number selection bits	Selects the transmit, test mode, and chip enable for the associated port number (00 through 15)
PNX1,2,4,8	Port number selection bits from the expansion BCLA	Port number from priority encoder of expansion BCLA to designate the active receive channel in the priority sequence
RSTPEL	Reset priority encoder latch	Resets the priority encoder latch after the receive channel of a port has been serviced
SYNCLK	Synchronous clock (6 MHz)	Synchronizes the expansion PWA to the primary PWA
SET-TM	Set test mode	Strobes the test mode decoder of expansion BCLA when PNR 8 bit is high
BRCLK	Baud rate clock	Provides 4.9152 MHz clock pulses to the baud rate generators, from which the baud rates are generated
DATA BUS	Eight data lines	The parallel data bus lines between the ports and the common controller
RXRDYX	Expansion BCLA receiver ready	Input to the primary BCLA priority encoder to indicate that an expansion BCLA receive channel requires servicing
TXRDYX	Expansion BCLA transmitter ready	Input to the primary BCLA to indicate that an expansion transmit channel requires service

COMMON CONTROLLER

The common controller contains the nucleus for many peripheral controller applications. This common controller comprises an eight-bit micro controller that is controlled by a firmware program of 256 64-bit instruction words. Each instruction word is composed of two 32-bit instruction words that are designated upper and lower. These upper or lower 32-bit instructions can be enabled independently or in sequence. One instruction is executed every 167 nanoseconds. The micro controller interfaces with the central processor unit (CPU) via input/output (A/Q) bus and direct memory access (DMA) bus to facilitate the communication link with network BCLA devices.

The common controller (figure 4-2) consists of an arithmetic logic unit (ALU), two general-purpose registers (L1 and L2), DMA data input register, file address, file register, bit generator, two selectors (S1 and S2), A/Q data and address registers, DMA data and address registers, timing, control, and firmware logic elements that function together as a micro processor (also referred to as a micro controller) under control of the firmware program. The ALU performs 16 different logic operations under control of the firmware ALU operation field and six arithmetic operations under control of the ALU operation field and F1 field selection. The ALU A inputs are from selector 1 (S1 bus), and the B inputs are from selector 2 (S2 bus). The ALU bus couples revised ALU data to the L1 and L2 registers, file address register, and the communication interface. The buffer inverters provide the signal inversion and signal buffering required by the A/Q and DMA registers.

The general-purpose registers provide operation sequencing, comparison testing, accumulation, and other functions required for the micro program designated process.

The two general-purpose registers are parallel-loading, eight-bit registers that provide three-state outputs. The L1 register feeds selector S1, which inputs to the A side of the ALU. The L2 register feeds selector 2 and the file register. Selector S2 inputs to the B side of the ALU via the S2 bus. In addition to the L2 register being parallel-loaded, the inputs may also be shifted left or right under control of the firmware F1 field. The file register is a 1024-byte (eight-bit) file that provides buffered storage of data from the L2 outputs in the locations specified by the file address register. This file feeds selector S1 to input stored data to the A side of the ALU.

A bit generator provides the insertion of single bits into selector S2 under the control of firmware field F1. The S1 and S2 selectors provide selection of their associated inputs to their respective three-state buses under the control of the firmware. These S1 and S2 buses feed the ALU control and data from the CPU and communication interface. The S1 bus carries read data, read status, status, and arithmetic and logic operands to the ALU A input. The S2 bus carries only arithmetic and logic operands to the ALU B input.

The A/Q and DMA data transfers are processed by the DMA data input register, selectors S1 and S2, and the A/Q and DMA address and data registers. The lower eight bits of the Q register are coupled to the ALU via selector S2 to determine the effective port and command. If a write command has been received, the A-register port control is coupled to the ALU via selector S1 and from the ALU to the communication interface. If the Q command is a read operation, the A-register data (BCLA identification or port identification) and status are packed in the A-data register under control of the firmware destination field and multiplexed along with other I/O device data to the processor via the I/O-TTY controller. DMA data from the processor is parallel-loaded (16 bits) into the DMA data input register under the control of a signal from the DMA. The data is placed eight bits at a time on the S1 three-state bus under the control of the firmware S1 field. The DMA address (16- to 20-bit) and data (16-bit) words are packed eight bits at a time into the respective holding register. This packing is accomplished under control of the firmware F2 field. These 16-bit words are multiplexed with other DMA devices and placed on the DMA bus.

COMMUNICATION INTERFACE

The communication interface provides control and data transfer logic for one to sixteen RS232-C-compatible communication lines between modems or terminals. The primary BCLA printed wiring assembly provides six communication ports. With the addition of an expansion BCLA printed wiring assembly, the capability is expanded to 16 communication ports. The primary controller is equipped with external interrupt gating that permits the integration of two to eight BCLA controllers, thus allowing for BCLA subsystem capability of six to 128 communication ports per macro interrupt.

Communication transfer may be via direct-coupled RS232-C voltage mode to modem or terminal located up to 500 feet (152 meters) from the controller, or communication transfer may be via converter-coupled RS232-C to 20 mA current loop to modem or terminal located up to 2000 feet (608 meters) from controller. The voltage mode to current loop conversion is accomplished by current loop adapters. These adapters are optical isolators that provide isolation through optical sensing (LED to photoelectric pickup).

Primary BCLA

The primary BCLA contains six communication ports and communications interface logic for control of sixteen ports. Character transfer between the modem(s) and communication port is accomplished in serial format of 7, 8, 9, and 10-bit character format. This format consists of character length (5, 6, 7, or 8 bits); parity bit (odd, even, or none); and stop time of one, one and one-half, or two bits. The communication port (Universal Synchronous/ Asynchronous Receiver/Transmitter, USART) converts serial data to parallel data during receive mode (read), and parallel data to serial data during transmit mode (write). The parity and stop bits are extracted from the character byte, by the USART during reads and are added to the character byte by the USART during writes.

During reads the character bytes are parallel-loaded on the bidirectional data bus lines and coupled via the data/interrupt selector to the S1 bus. The S1 bus couples the data to the A input of the ALU for modification or transfer via the DMA registers to the processor main memory. During writes the character byte from the ALU is parallel-loaded via the port data latch into the USART. The USART then transmits the character in serial format.

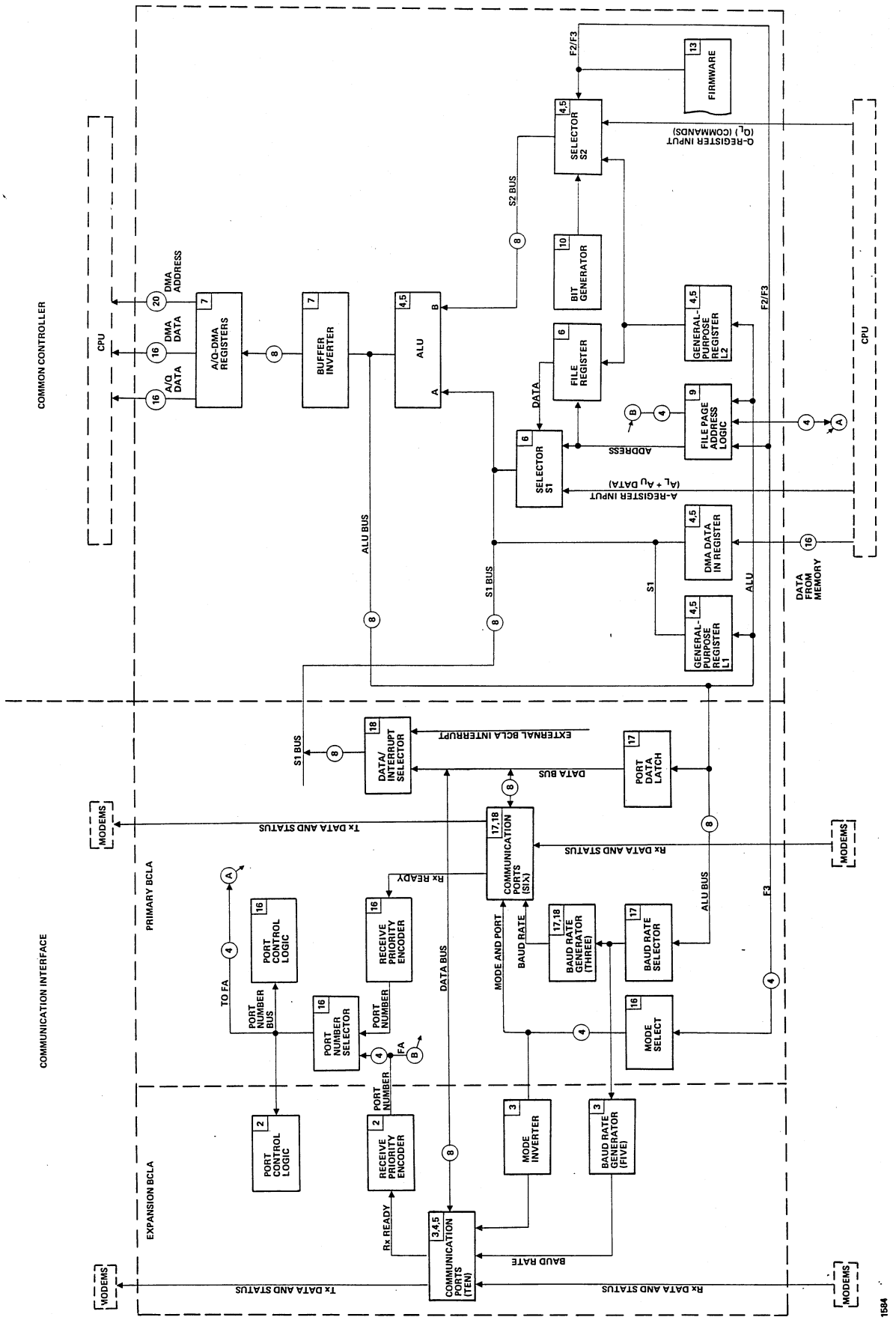


Figure 4-2. BCLA Controller Block Diagram

All reads and writes are asynchronously coupled from and to the terminal(s) at baud rates compatible to the terminal. The baud rate selector produces a baud rate code that determines the transfer baud rate. The baud rate code is derived from the ALU upper four bits (ALU4-7). This code can select 16 different baud rates. Data may be transferred in half duplex or full duplex. The baud rate for receive and transmit is always the same.

The mode selection logic selects the BCLA port and designates the mode (read or write) and the content (control or data) of the character byte. These selections are determined by the F3 field of the firmware.

The port control logic, under the control of the file page address logic and the receive priority encoder, determines the active port. The conditions of the port number bus designate one of six ports of the primary BCLA or one of ten ports of the expansion BCLA. During read operations the receive priority encoder designates the lowest numbered active port that requests service. During write operations the file page address designates the active port in accordance with the firmware scan routine.

Expansion BCLA

The expansion BCLA increases the communication port capability of a BCLA subsystem by an additional ten ports. The ports of the expansion BCLA function identically to the primary BCLA ports, and all ports are transparent to the processor except the active port. Baud rate and mode and port control are selected and controlled from the primary BCLA. The priority encoder output is combined with the primary BCLA priority encoding, and selection is designated with highest priority to the lowest numbered port.

DETAILED FUNCTIONAL DESCRIPTIONS

The following detailed functional descriptions are arranged in three categories: descriptions applicable to the overall controller, those applicable to the common controller, and those applicable to the communication interface. The overall controller descriptions include the timing and master clear. The common controller descriptions include data path, control signal selection, DMA control, and A/Q control. The communication interface descriptions include command, status, data, and control selections.

OVERALL CONTROLLER

These descriptions include functions that are applicable to both the common controller and the communication interface.

Timing Generator

The timing generator (figure 4-3) produces the timing pulses that clock the communication interface control operations and the common controller data and control operations. The common controller data operations include the A/Q and DMA data and address registers, general-purpose registers L1 and L2, and the file address counter. The control operation includes the auxiliary condition selector latches, the F1 strobes selector, and the instruction address counter. The communication interface data and control operation include the priority encoder, the F2 strobe decoder, and the baud rate code latch.

The source of the clock pulses is a 12.0 MHz crystal oscillator. The 12.0 MHz signal is gated with the stop-the-clock enable and the external (EXT) enable at AND gate U23 and OR gate U25. When stop the clock is active, the external trigger input OR gate is enabled to permit timing generation from an external source. The OR gate output produces two clock states (CLK and CLK/) that clock the 6.0 MHz clock generator, the file write register, and the clock generator gating. The clock (CLK/) pulse chain is divided by 2 and NANDed with the clock high signal to produce the 6.0 MHz (A-TCK, TCLK, TCLK-2, and TCLK-3) pulses. These time clock pulses (TCLK, -2, and -3) are applied to the common controller; the A-CLK pulse chain is applied to the communication interface. The TCLK/ and CLK/ pulse chains are also made available for external use at backplane terminals (80 and 81, respectively).

The write enable ($\overline{WE}$) signal is generated when the firmware destination field selects L2F active. This active L2F condition is gated to the register on the next low clock pulse. The register output then enables the file write register latch, which activates the write enable (WE) on the low-to-high transition of 12.0 MHz clock (CLK) pulse.

A master reset (MR/) signal from the I/O-TTY controller stops the 6.0 MHz clock generator. When the master reset is removed, the 6.0 MHz generator output resumes.

6 MHz Clock Generator

The 6.0 MHz clock generator is enabled and disabled by the output of AND gate U42. When the TEST, master reset, and divide-by-2 latch output at U64-6 are high, the output of AND gate U42 applies a high to the input of the divide-by-2 latch. On the next high-to-low transistion of the clock (CLK/) pulse, the outputs change (U64-6 low, U64-7 high). The low output of U64-6 toggles the output of AND gate U42, and the high state of U64-7 enables the output AND gates (U66 and U75). On the following low-to-high transition of the clock pulse (CLK/), the output AND gates are activated to produce the time clock ($\overline{A\text{-}TCLK}$, $\overline{TCLK}$, $\overline{TCLK\text{-}2}$, and $\overline{TCLK\text{-}3}$) pulse outputs. (Refer to the timing diagram in figure 4-3.) The next high-to-low CLK/transition alternates the outputs of the divide-by-2 latch to disable the output gates that drive the TCLK line high.

File Write Register

The write enable (WE) pulse is produced when specified by the firmware destination field. The destination field drives the latch L2 and file (L2F) signal low. (During the next TCLK cycle following the L2F selection, the write enable occurs.) This L2F low enables AND gate U55. Then the next time that clock/2 frequency is low, AND gate U55 is activated. This enables the write register (U64-10, -11, and -12). At the next high-to-low transition of the clock (CLK/) pulse, the high output at U64 pint 10 enables the file write register U65. With U65 enabled, the next clock pulse transition (low to high) activates U65; and the file write enable low occurs. This write enable low occurs 41.6 nanoseconds after the instruction time starts, and after TCLK, and remains low for 83.6 nanoseconds until the clock pulse goes low. This write enable low (WE) signal then strobes the register file (U83 through U90).

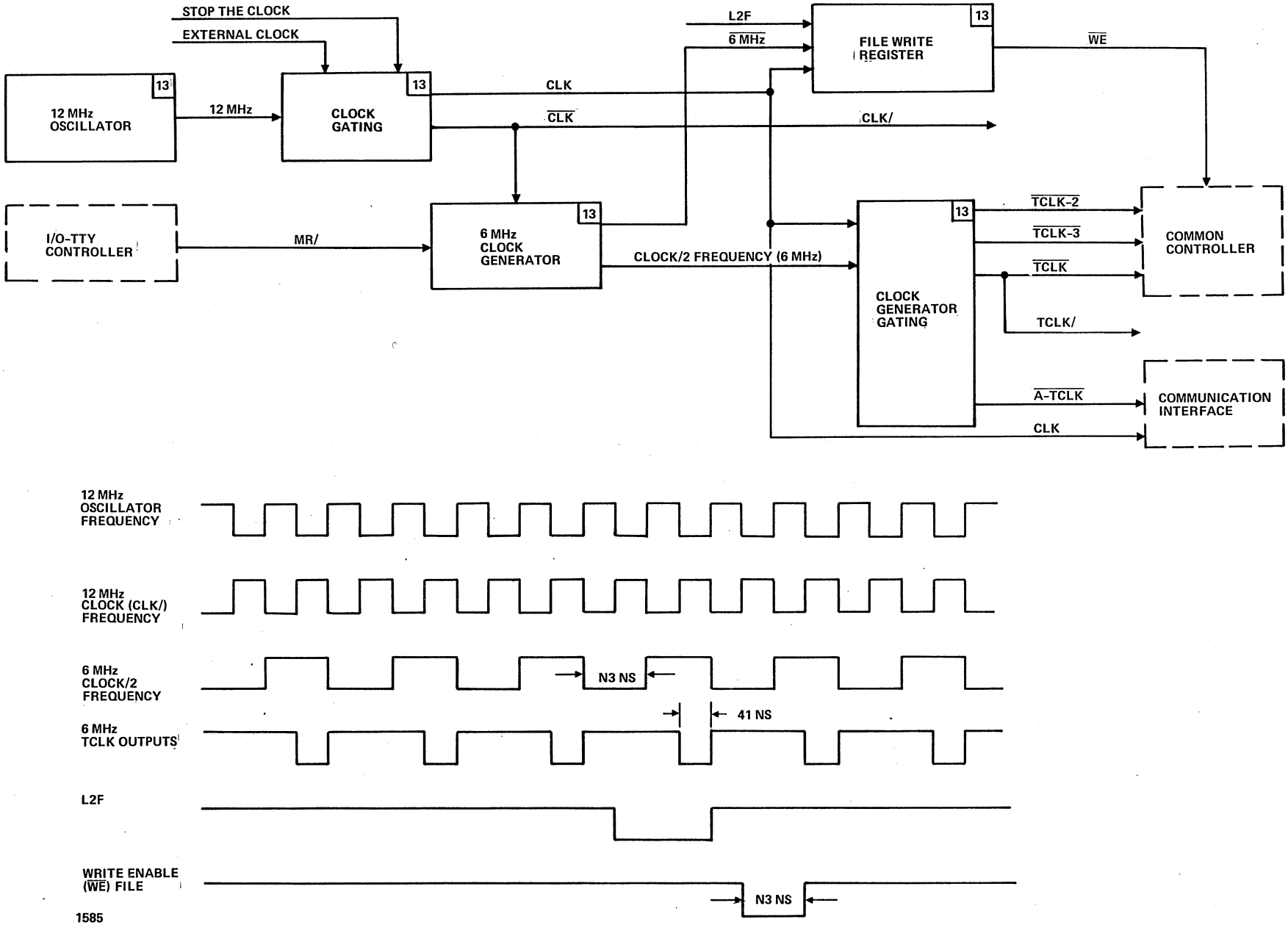


Figure 4-3. Timing (Clock) Generator

Master Clear

The master clear function (figure 4-4) provides the master clearing of the common controller and the communication interface and the inhibiting of the timing generator. The master clear operation is activated when the master reset (MR/) input from the I/O-TTY controller goes active. This produces the master clear ($\overline{MC}$) low signal that resets the auxiliary condition latch, the control bits 1 register, and the instruction address counter; this signal disables the DMA enable latch of the common controller. This master clear low is also ORed with +5 V dc. When either signal is active (MC or loss of +5 V dc), an (IACLR) is applied to the instruction address counter and auxiliary condition latch. The master clear ($\overline{MC}$) also clears the channel mode latch and loop test mode decoders of the communication interface (primary and expansion BCLAs). In addition, the master clear resets ROM address to enable execution of the firmware master clear routine.

When the master reset signal at backplane terminal 46 goes active, the master clear latch of register U64 is enabled. At the next high-to-low transition of the timing generator clock (CLK/) pulse, the master clear (MC) signal goes low. This master clear low disables AND gate U42 to inhibit the time generator output. The resulting master clear (MC) resets the common controller and communication interface.

COMMON CONTROLLER

The common controller occupies approximately two-thirds of the printed wiring assembly (see figure 1-1). It contains the micro-controller elements that provide a data and control communication link between the communication interface and the central processor. The control interface with the central processor is provided via the input/output (A/Q) bus, and the data interface is provided via the direct memory access (DMA) bus.

The data path (figure 4-5) routes 8-bit bytes of data to and from the communication interface and the central processor. The heart of data transfer is the arithmetic logic unit (ALU), which is capable of performing 16 different logic operations and six arithmetic operations under control of the firmware ALU and F1 fields.

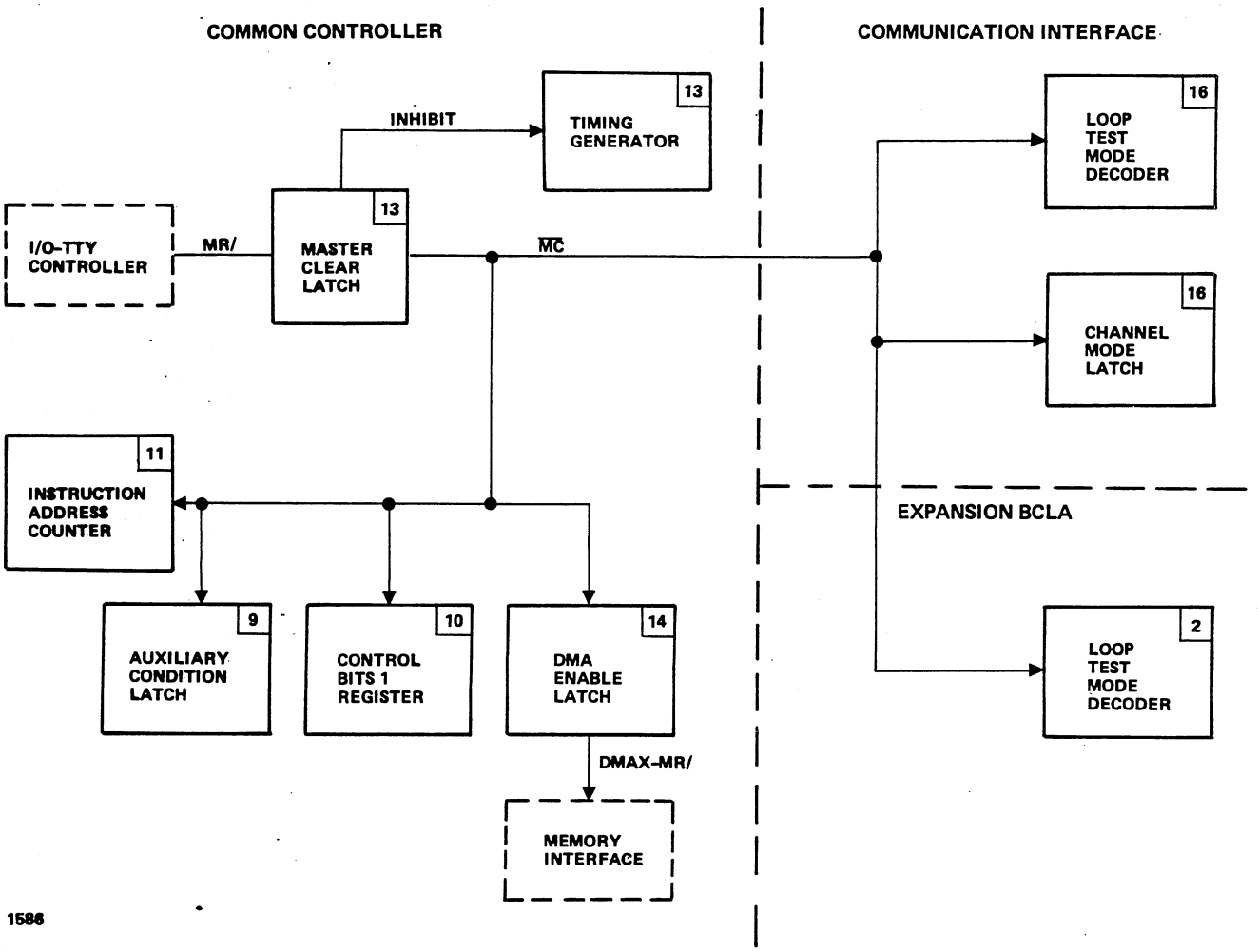
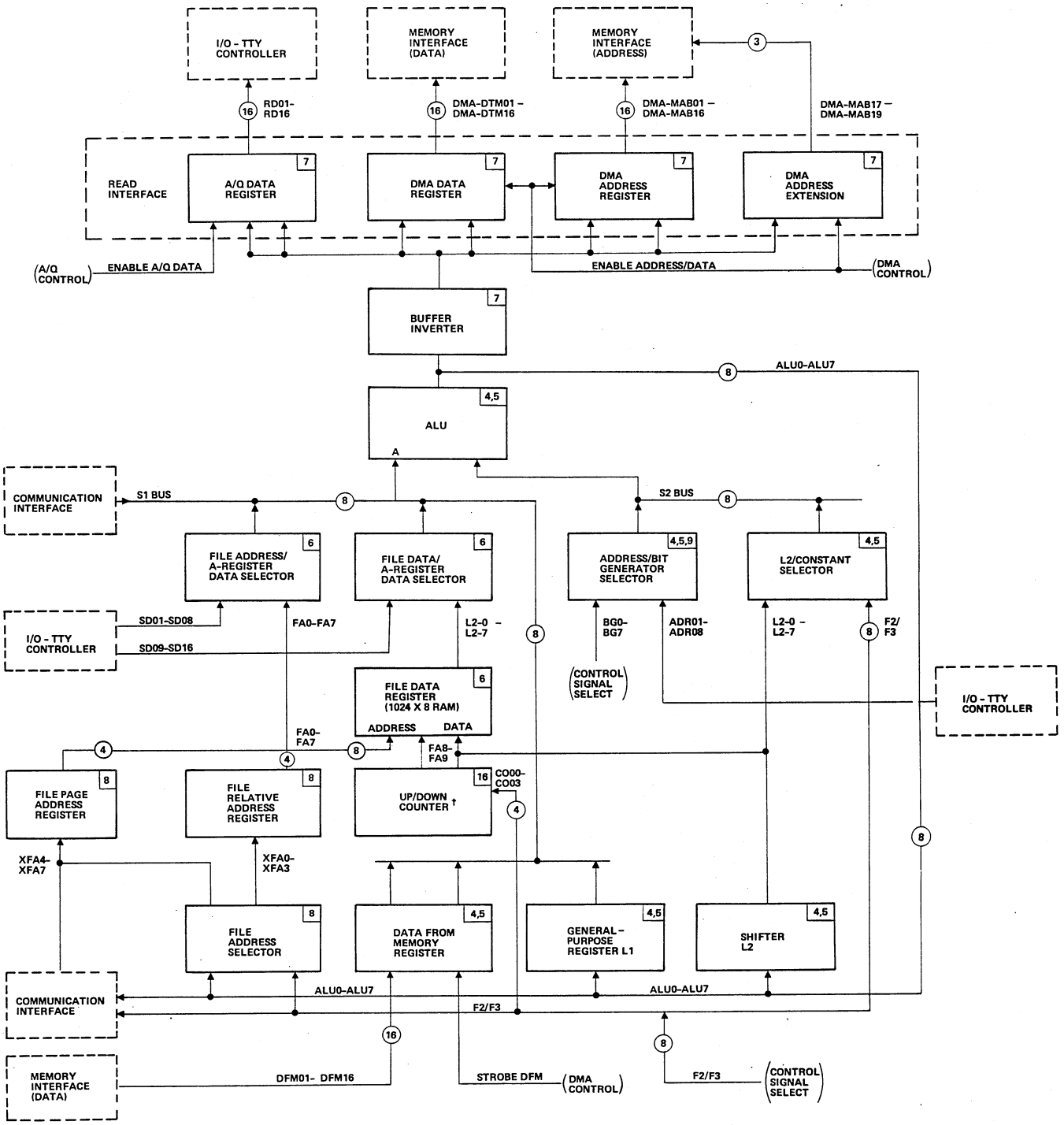


Figure 4-4. Master Clear Functional Block Diagram



†PART OF COMMUNICATION INTERFACE LOGIC COMPONENTS

1587

Figure 4-5. BCLA Common Controller Data Path

Arithmetic operations are enabled when the F1 field equals 2 or 3 (figure 4-6). These logic and arithmetic operations are performed on the S1 and S2 bus conditions existing at ALU inputs A and B. The ALU data outputs feed the buffer inverters, general-purpose registers L1 (U98 and U103), shifter L2 (U97 and U102), the file address selector (U49 and U50), and the communication interface. The ALU buffer inverters prevent overloading of the ALU outputs and provide correct data polarity to the direct memory access (DMA) and A/Q data registers. These registers facilitate the DMA and A/Q data transfer from the communication interface to the central processor via the CPU's memory interface and I/O-TTY controller.

Data bytes are transferred from the communication interface via the S1 bus and the ALU to the file register (U83 through U90) buffer area. The data word (16 bits) is assembled byte by byte, with the upper byte (bits 19 through 16) first and the lower byte (bits 1 through 8 last. After the word is assembled, the DMA data word is packed into DMA data registers (U124 and U136) under the control of the load data upper and load data lower strobes. The address word is packed into the DMA address registers (U123, U134, and U135) under the control of the load memory address upper, load memory address lower, and load memory address high. The DMA data words are transferred to the processor main memory address designated by the memory address bits under the control of the processor DMA.

In the A/Q mode, commands, identification (port and BCLA), and status words are transferred from the communication interface and packed byte by byte into a buffer area of the register (U83 through U90). The processor input to A instructions initiates the transfer of data (word by word, 16 bits per word) from the file register. Under the control of the firmware destination field, the upper and lower bytes of each word are then loaded into the A/Q data register. This register has three state outputs to allow multiplexing with other I/O devices. When the CPU read line becomes active, the data is placed on the bus.

DMA data from the CPU main memory is unpacked word by word (16 bits) into the data from memory (DFM) register (U125 and U137). Each data word is then transferred byte by byte from the DFM registers to the file register via the S1 bus, the ALU, and general-purpose register L2. The DMA data is stored in the file address designated by the file address selector (U49 and U50), the file page address register (U60), and the file relative address register (U61).

A/Q data from the CPU via the I/O-TTY controller is packed byte by byte into the file register buffer area via the S1 bus selectors (upper byte U99 and U104, and lower byte U100 and U105), the ALU (U95 and U96), and shifter L2 (U97 and U102). This A/Q packing is under the control of the firmware via the file address selector.

Address bits (ADR01 through ADR08) applied to the address/bit generator selector (U69 and U70) designate the command code that defines the controller operation (see section 2). The bit generator (U71) inputs (BG0 through BG7) allow for the insertion of single bits into the ALU via the S2 bus.

The combined F2/F3 firmware field operations are considered as one 8-bit field. When applied to the file address selector (U49 and U50), they designate the direct file address. When applied to the L2/constant selector (U81 and U82), they provide constants required by the firmware.

The shifter L2 (U97 and U102) is general-purpose, 8-bit register that parallel-loads data from the ALU, or serially shifts data from right to left or left to right under the control of the S0 and S1 mode selectors. When both the S0 and S1 mode selectors are high, data is parallel-loaded and serial inputs are inhibited. The ALU data is then placed on the output lines when the time clock (TCLK) signal goes positive. This output data is parallel-coupled to the S2 bus via the L2/constant selector (U81 and U82), parallel-coupled to the file data input, and serial-coupled to its own left and right serial inputs. These serial inputs provide for shifting L2 under control of the F1 field. When the S0 input is high, the shift right is enabled; and data is shifted synchronously with the trailing edge of clock pulse. When the S1 input is high, the shift left is enabled.

S2 Bus

The S2 bus is a three-state bus that places the Q-register command, bit generator, shifter (L2), or constants (F2/F3) on the ALU B input. These inputs are obtained from either of two multiplexers. One multiplexer (address or bit generator selector) consists of two two-to-one, inverting multiplexers; and the other (L2 or constant selector) consists of two two-to-one, noninverting multiplexers.

L2/Constant Selector

This L2/constant selector (U81 and U82) is a two-to-one, noninverting multiplexer included in selector S2. This selector provides for selection of the shifter L2 data or the firmware F2/F3 field bits. It also provides three-state output and input selection. When the output control signal C18 is high, this selector's output lines are at high impedance. When the output control signal C18 is low and the select control signal C17 is high, the 0 inputs (constants from the F2/F3 field bits) are applied to the S2 bus. When the output control signal C18 is low and the select control is low, the 1 inputs (shifter L2 data) are applied to the S2 bus.

Address/Bit Generator Selector

This selector (U69 and U70) is an eight-bit, inverting multiplexer that determines which input (address data on 1 or bit generator data on 0) shall be placed on the S2 bus. The complement of the Q-register command bits (ADR01 through ADR08) are placed on the S2 bus when C18 is low and C17 is high. The bit-generator bits are placed on the S2 bus when C18 and C17 are both low. When C18 is high, the outputs are at the high-impedance state.

S1 Bus

The S1 bus is a three-state bus that places communication interface inputs, A/Q data, file address, file data, DMA data from memory, or ALU update on the ALU A input. The selection of inputs to the S1 bus is determined by the firmware S1 field.

File Data/A-Register Data Selector

This selector (U99 and U104) is an eight-bit, noninverting multiplexer. It places the A-register eight bits (SD09 through SD16) or the file register data (eight bits) on the S1 bus. When the file A-register upper (FL-AU) signal and bit C23 of the S1 field are active (low), the A-register data bits are placed on the S1 bus. When the FA-AU signal is low and C23 is high, the file data bit conditions are placed on the S1 bus. When the FA-AU signal is high, the selector outputs are in a high-impedance state.

File Address/A-Register Data Selector

This selector (U100 and U105) is an eight-bit, noninverting multiplexer. It places the A-register eight bits (SD01 through SD08) or the file address eight bits (FA0 through FA7) on the S1 bus. When the file address A-register lower (FA-AL) signal and bit C23 of the S1 field are active (low), the file address bit conditions are placed on the S1 bus. When FA-AL is low and C23 is high, the A-register data bit conditions are placed on the S1 bus. When FA-AL is high, the selector outputs are in a high-impedance state.

General-Purpose Register L1

This register (U98 and U103) is a three-state, eight-bit, parallel-load, positive-edge-triggered register with two operating modes, parallel load or hold. When the destination field sets trigger latch 1 (TL1) active (low), the data present at the D inputs is loaded at the next low-to-high transition of the clock pulse (TCLK-2 and TCLK-3). The latch holds this data until signals, L1 and C23 from the S1 field, both become active (low). When they are active, the ALU0 through ALU7 bit conditions are placed on the S1 bus. When either L1 or C23 is high, the output of the latch is in a high-impedance state.

Data from Memory Register

The data from memory registers (U125 and U137) are parallel-loaded with data (16-bits) from the CPU main memory under the control of the S1 field and the DMA control cycle. The data is multiplexed onto the S1 bus one byte (eight bits) at a time by the enable signals $\overline{C23}$, C23, and $\overline{DFM}$. When the strobe data from memory (STB-DFM) signal, applied to the register clock input, goes positive, the data from memory bit conditions are parallel-loaded. These bits are held until released by the output control signal from AND gate U106. When the output control signal (F) is low, the data bit conditions are placed on the S1 bus. When the output control signal is high, the output is at high impedance.

The output control signal state is dependent upon the C23, $\overline{C23}$, and $\overline{DFM}$ inputs to AND gate U106. When C23 and DFM are active (low), the DFM01 through DFM08 data bits are placed on the S1 bus. When C23 and DFM are active (low), the DFM09 through DFM16 data bits are placed on the S1 bus. If either AND gate input is high, the output sends the register outputs to the high-impedance level.

Supplementary Data Elements

The supplementary data elements (registers and multiplexers) comprise the file address selector, file address counters (file page address and file relative address), and file register.

File Address Selector

The file address selector consists of two two-to-one multiplexers (U49 and U50) that select either the ALU or firmware F2/F3 field bits. The F2/F3 field bits are normally selected. The ALU bits are selected when the destination field designates the file address register. When the load file address ($\overline{LOAD\ FA}$) signal is high, the F3 field bits (C00 through C03) are selected to load the file relative address (FRA) counter; and the port number bits (PNR1, 2, 4, and 8) are loaded into selector U49. When the $\overline{LOAD\ FA}$ signal is low, the ALU bits (ALU0 through ALU3) are selected to load the file relative address counter; and the ALU bits (ALU4 through ALU7) are loaded into selector U49. The high-impedance state of selector U50 is not operational since the enable input is hard-wired to ground. When the enable file address multiplexer signal (EN-FAM) is active (low), the data held in U49 is placed on the file page address lines. When $\overline{EN\text{-}FAM}$ is inactive, the U49 output is at high impedance.

File Address Counter

The file address counter consists of two four-bit counters (U60 and U61) and an up/down counter (U3). One counter (U60) provides a four-bit address (FA4 through FA7) that designates one of sixteen pages. The other counter (U61) provides a four-bit address (FA0 through FA3) that designates one of sixteen locations within a designated page. The file page address counter can be incremented by the firmware F1 field. The file relative address counter can be incremented by firmware fields F1 and F2. When the load file address (LD-FA) signal from the destination decoder is active, the next positive transition of the clock presets both counters to the count designated by XFA0 through XFA7. When the increment signals (INC-FA and INCFPA) become active, the respective counter is incremented while the signal remains active. If the carry signal (FRAEQF or FAEQFF) becomes active, the main condition multiplexer (U33) effects a change in the firmware instruction.

The up/down counter provides address bits FA8 and FA9. These bits designate the file register segment within the page. Control bits C00 and C07 determine the preset condition of the counter. The selection F2 bits (C04 through C06) applied to the F2 strobes decoder (U4) designate count up or count down and clear to zero control.

File Data Register

The file data register comprises eight 1024-by-one-bit read/write memory chips (U83 through U90) to provide a file register of 1024 bytes. The memory is arranged in four

segments (00 through 03) of 256 eight-bit bytes. Each segment contains 16 pages, 0 through F; and each page contains 16 bytes of storage. The up/down counter bits FA8 and FA9 select the segment area. The file page address counter outputs FA4 through FA7 select the page, and the file relative address counter outputs FA0 through FA3 designate the byte location within the page.

Writes to the file data register are under the control of the firmware destination field (L2F) selection (refer to timing generator). Data is placed in the shifter at the end of the instruction, and the file write takes place during the next instruction when the write enable (WE) is active. Therefore, the file address (FA) may be set during the same instruction that specifies a file write. But a file read may not be accomplished in the instruction immediately following a file write because the writing is actually taking place at that time. When reading the file, the file address must be set to the desired address at least one instruction before the file is read.

A write is enabled when WE is low; a read is enabled when WE is high. The data is stored in the designated file address during write enables, the data is retrieved from the designated file during a read enable.

Arithmetic Logic Unit (ALU)

The ALU is comprised of two four-bit ALU function generators (U95 and U96) to provide logic and arithmetic operations of eight-bit bytes. The ALU performs 16 logic operations (figure 4-6) under control of the firmware ALU field. In addition, the ALU performs six arithmetic operations under control of the firmware ALU and F1 fields. The A inputs are obtained from the S1 bus. The B inputs are obtained from the S2 bus. The output (ALU0 through ALU7) is applied to the buffer inverters, general-purpose register L1, shifter L2, the file address selector, and the communication interface.

The logic operations are selected by the firmware ALU field (C19 through C22) logic states applied to the four function selection inputs (1, 2, 4, and 8) when the mode select (M) input is high. The arithmetic operations are selected by the function select inputs (C19 through C22) when the mode select (M) input is low. The comparison (AUEQFF) operation is decoded from the output signals ALU0 through ALU7. When words of equal value are present at the A and B inputs, the ALU equal FF (AUEQFF) assumes a high level to indicate the equality (A = B).

Read Interface

The read interface is comprised of the A/Q data register, the DMA address register, and the DMA data register. The A/Q data register transfers data (status) word by word to the A register of the central processor via the I/O-TTY controller. The DMA data register transfers character data word by word to the central processor main memory locations designated by the DMA address.

A/Q Data Register

The A/Q data register comprises two eight-bit, three-state, D-type registers (U120 and U132). These registers provide a 16-bit buffer data latch that permits data to the CPU A register to be multiplexed with the other I/O devices. The latches are parallel-loaded one byte at a time from the ALU buffer inverters under control of the firmware destination field. When the A/Q data upper (ATU) signal is low, the upper data byte is loaded into the upper A/Q data registers (U120) on the next low-to-high transition of the clock (TCLK-3) pulse. When the A/Q data lower (ATL) signal is low and TCLK-3 goes from low to high, the lower data register (U132) is loaded. This data is held in the registers until the enable A/Q data (E-A/Q-DATA) signal goes active (low) to place the data held in both registers on the read lines (RD01 through RD16). When the E-A/Q-DATA signal is high, the output lines are in the high-impedance state. These registers store the complement of the ALU output, as produced by buffer inverters U132 and U133.

DMA Address Register

The DMA address register comprises three (two 8-bit and one 4-bit) three-state, D-type registers (U123, U135, and U134). The three-state output permits the address to be multiplexed with other DMA devices. The latches are parallel-loaded one byte at a time, upper byte first, under the control of the load DMA upper, lower, and high signals derived from the firmware F2 field. When the load DMA upper ($\overline{\text{LDDMAU}}$) signal is low, the upper address byte is loaded into the upper DMA address register (U123) on the next low-to-high transition of the $\overline{\text{TCLK-3}}$ pulse. When the load DMA lower ($\overline{\text{LDDMAL}}$) signal is low, the lower address byte is loaded into the lower DMA address register (U135) on the next low-to-high transition of TCLK-3 pulse. When the load DMA high (LDDMAH) signal is low, the high address is loaded into the high DMA address register (U134) on the next low-to-high transition of TCLK-3. The DMA address is retained in the DMA address registers until the enable additional data (E-ADD-DATA) signal goes active to place the address bits on the DMA-MAB 01 through DMA-MAB 17 and DMA-MAB 19 lines. When E-ADD-DATA signal is high, the output terminals of the registers are in the high-impedance state. These registers hold the complement of the ALU output.

DMA Data Registers

The DMA data registers comprise two eight-bit, three-state, D-type registers (U124 and U136). Data is loaded in the same manner as the DMA address registers by the load data upper and lower signals ($\overline{\text{LDDTU}}$ and $\overline{\text{LDDTL}}$, respectively). The stored data is the complement of the ALU output, Data is released during the low state of the enable address and data ($\overline{\text{E-ADD-DATA}}$) signal, under the control of the CPU DMA facilities.

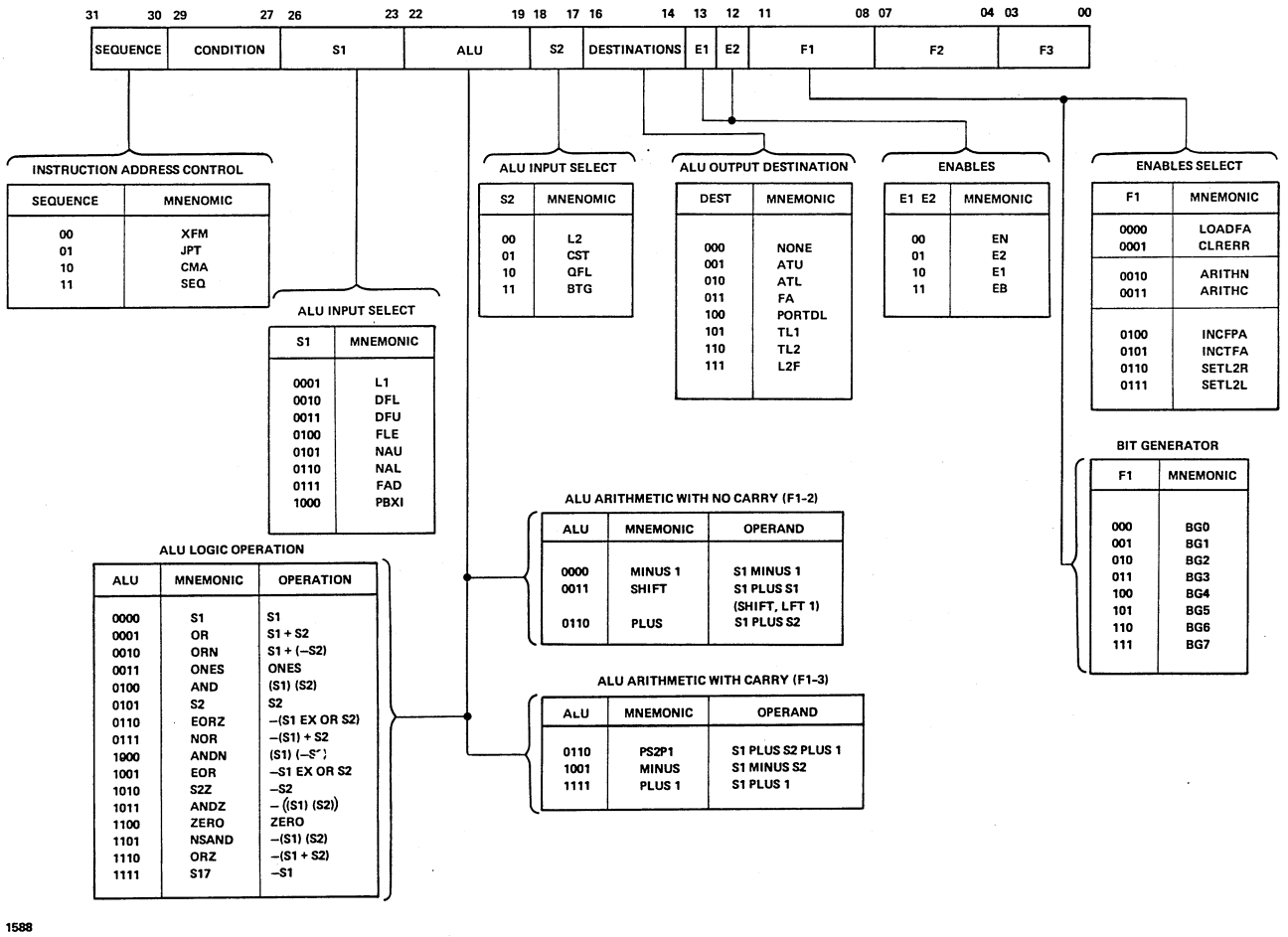


Figure 4-6. ALU Operations

Control Path

The control path (figure 4-7) comprises the firmware, selectors, decoders, and latches of the common controller that function logically to control data flow between the controller's processor, the communication interface, and the CPU. The firmware contains the control program of 512 64-bit words. These words are released as 32-bit instructions (designated upper and lower) by the instruction address selector and expansion register. These 32-bit instructions program the operation and data flow of the common controller and communication interface. Instruction addresses are derived from either the F2/F3 (C00 through C07) field bits, or the output of the ALU (ALU0 through ALU7), or by incrementing the instruction address under control of the sequence field bits (C30 and C31). The auxiliary and main condition selectors, controlled by the condition field, designate that the upper or lower 32-bit instructions of the 64-bit word shall provide the next instruction selected by the instruction address. The F2/F3 field bits designate the jump address, and the ALU bits designate the transform address.

Firmware

The firmware provides the BCLA controller micro instructions that are contained in four 1024, eight-bit, read-only memory (ROM) chips (U19 through U22). These ROMs are combined and formatted to provide a 512-word (64 bits each) program (Appendix B) that controls all operations and data transfers performed by the BCLA subsystem. Each word is divided into two 32-bit instructions (designated upper and lower), thus providing 1024 32-bit micro instructions. The instruction address designates the program word, and the lower signal high or low conditions select the upper and lower instruction.

Each micro instruction contains 11 control fields (figure 4-7): sequence, condition, S1, ALU, S2, destination, E1, E2, F1, F2, and F3. The sequence field (bits 31 and 30) controls the loading and incrementing of the instruction address (table 4-3) to select one of four instruction sequences. The condition field selects the inputs to the main condition selector. The selected condition (table 4-4) determines which instruction word (upper or lower 32 bits) is to be utilized next. The S1 field selects the inputs to the

TABLE 4-3. SEQUENCE FIELD CONTROL

Sequence Field Bits		Mnemonic	Action
31	30		
0	0	XFM	Load ALU bits into instruction address
0	1	JPT	Load F2/F3 bits into instruction address
1	0	CMA	Do not change instruction address
1	1	SEQ	Increment instruction address

TABLE 4-4. CONDITION FIELD CONTROL

Condition Field Bits			Mnemonic	Action
29	28	27		
0	0	0	LOWER	Hardwired low (tied to ground)
0	0	1	UPPER	Hardwired high (tied to high, HI-1)
0	1	0	AUX1	Select auxiliary 1 condition (table 4-9)
0	1	1	FREAEQF	File relative address equals F_{16} (beginning of current instruction)
1	0	0	AUEQFF	ALU output equals F_{16} (A inputs = B inputs) (end of current instruction)
1	0	1	FPAEQF	File page address counter equals F_{16} (beginning of current instruction)
1	1	0	CYNOT	No carry from ALU (end of current instruction)
1	1	1	RxRDYN	Receiver N (00 through 15) has data ready

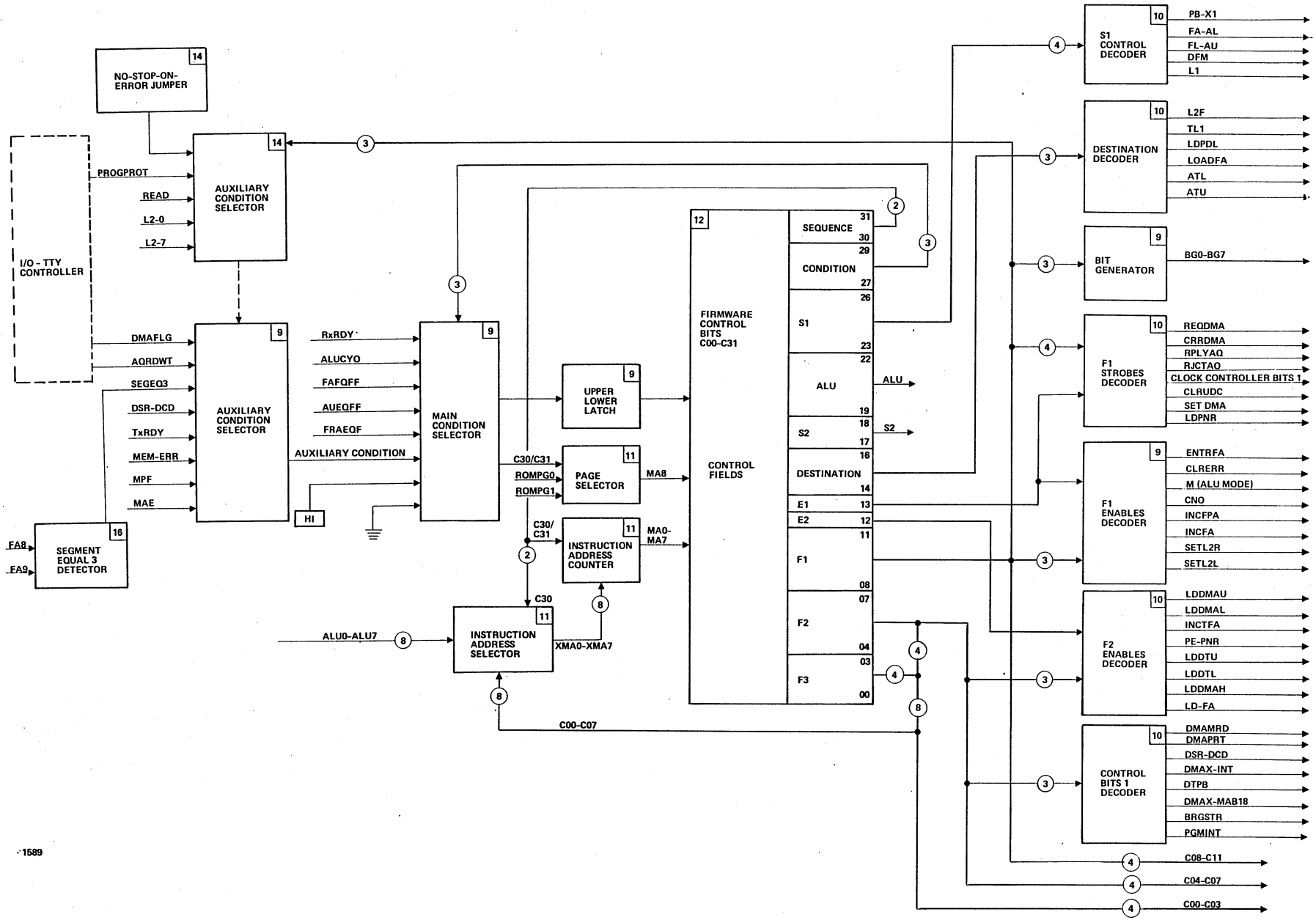


Figure 4-7. BCLA Common Controller, Control Signal Selection

A input of the ALU via selector S1 (table 4-5). The ALU field provides the selection inputs to the ALU to designate the operating function (table 4-6). These inputs select one of 16 logic operations or one of six arithmetic operations when designated by the F1 field. The S2 field selects the inputs to the B input of the ALU via selector S2 (table 4-7). The destination field designates the destination of the ALU output: L1 latch, L2, A/Q data register, communication interface, or file (table 4-8). The E1 and E2 bits enable or inhibit the F1 and F2 enable and strobe selectors (table 4-9). Since the F1 field is used for other purposes, the E1 bit provides a method of selecting the strobes and enables. The F1 field provides the select address for the F1 strobes, F1 enables, bit generator output, and communication interface conditions via the auxiliary operations selectors (table 4-10). The F2 field (table 4-11) combines with the F3 field to provide the program jump controls applied to the instruction address selector. In addition, the F2 field also provides bits to control the up/down counter and port control registers of the communication interface. The F3 field controls the operations of the communication ports and preset of up/down counter and provides constants to the common controller.

The F2/F3 combination field is considered as one eight-bit field that provides instruction addresses, file addresses, and ALU constants.

Instruction Address Counter

The instruction address counter (U27 and U28) provides the primary address bits to the firmware control memory. These address bits, MA0 through MA7, combine with the page select address bit MA8 to select one of 1024 32-bit instructions residing in page 0 or 1 of the control memory.

The instruction address may be derived from the lower eight bits (F2/F3) of the control memory instruction, the eight-bit output of the ALU (ALU0 through ALU7); or it may be derived by incrementing the address bits contained in the instruction address counter. When control bit C30 is low and C31 is high, the instruction address does not change for implemention of the upper instruction to the lower instruction; the change is accomplished by the LOWER signal state. When C30 and C31 are both low, the ALU bits determine the instruction address. When C30 is high and C31 is low, the F2/F3 bits determine the instruction address. When C30 and C31 are both high, the instruction address is incremented. The operation of the instruction address counter is strobed by the low-to-high transition of the clock pulse ($\overline{TCLK}$).

Instruction Address Multiplexer

The instruction address multiplexer comprises two two-to-one multiplexers (U38 and U39). Data input to these multiplexers is from the control instruction field (F2/F3) bits and the ALU output. When sequence field bit C30 is low, the ALU bits provide the instruction address. When the C30 bit is high, the F2/F3 field bits (C00 through C07) provide the instruction address. The output control selection terminal is hardwired to low state, thereby disabling the three-state operation of these multiplexers.

Main Condition Selector

The main condition selector (U33) is an eight-to-one multiplexer that controls the output of the upper/lower instruction selector (U63). When the instruction selector is active, the lower 512 instruction set is enabled. When

TABLE 4-5. S1 FIELD CONTROL

S1 Field Bits				Mnemonic	Action
26	25	24	23		
0	0	0	1	L1	General-purpose register L1 output enabled.
0	0	1	0	DFL	Enable output from data from memory lower register.
0	0	1	1	DFU	Enable output from data from memory upper register
0	1	0	0	FLE	Select transfer of file data to S1 bus.
0	1	0	1	NAU	Select transfer of A/Q data upper to S1 bus.
0	1	1	0	NAL	Select transfer of A/Q data lower to S1 bus.
0	1	1	1	FAD	Select transfer of file address to S1 bus.
1	0	0	0	PBXI	Select communication port bus or external interrupts from additional BCLA controller

TABLE 4-6. ALU FIELD CONTROL (LOGIC OPERATIONS)

ALU Field Bits				Logic Operation	Action
22	21	20	19		
0	0	0	0	S1	S1
0	0	0	1	OR	S1 + S2
0	0	1	0	ORN	S1 + (-S2)
0	0	1	1	ONES	ONES
0	1	0	0	AND	(S1) (S2)
0	1	0	1	S2	S2
0	1	1	0	EORZ	-(S1 EX. OR S2)
0	1	1	1	NOR	-(S1) + S2
1	0	0	0	ANDN	(S1) (-S2)
1	0	0	1	EOR	S1 EX. OR S2
1	0	1	0	S2Z	-S2
1	0	1	1	NAND	- (S1) (S2)
1	1	0	0	ZERO	ZERO
1	1	0	1	NS1AND	-(S1) (S2)
1	1	1	0	ORZ	-(S1 + S2)
1	1	1	1	S1Z	-S1
Arithmetic Operation Without Carry†					
0	0	0	0	MINUS	S1 minus 1
0	0	1	1	SHIFT	S1 plus S1 (shift left 1)
0	1	1	0	PLUS	S1 plus S2
Arithmetic Operation with Carry††					
0	1	1	0	PS2P1	S1 plus S2 plus 1
1	0	0	1	MINUS	S1 minus S2
1	1	1	1	PLUS1	S1 plus 1

†When field F1 equals 2

††When field F1 equals 3

TABLE 4-7. S2 FIELD CONTROL

S2 FIeld		Logic Operation	Action
18	17		
0	0	L2	Select shifter L2 bits to S2 bus
0	1	CST	Select F2/F3 field bits to S2 bus
1	0	QFL	Select Q-address bits ADR0 through ADR08 to S2 bus
1	1	BTG	Select bit generator to S2 bus

TABLE 4-8. DESTINATION FIELD CONTROL

Destination Field			Mnemonic	Action
16	15	14		
0	0	0	NONE	No destination selected
0	0	1	ATU	Enable loading of A/Q data register/ upper
0	1	0	ATL	Enable loading of A/Q data register/ lower
0	1	1	FA	Enable loading of file address
1	0	0	PORTDL	Enable loading of port data latch and baud rate code latch
1	0	1	TL1	Enable loading of general-purpose register L1
1	1	0	TL2	Enable loading of shifter L2
1	1	1	L2F	Enable loading of shifter L2 and write to file

TABLE 4-9. E1 AND E2 ENABLES FIELD CONTROL

E1 and E2 Field Bits		Mnemonic	Action
13	12		
0	0	EN	Neither field F1 or F2 enabled
0	1	E2	Enable field F2
1	0	E1	Enable field F1
1	1	EB	Enable both field F1 and F2

TABLE 4-10. F1 FIELD CONTROL

F1 Field Bits				Mnemonic	Action
11	10	9	8		
F1 Field Enables					
0	0	0	0	LOADFA	Load file address register (F2/F3 bits to file address)
0	0	0	1	CLRERR	Clear error; DMA protect fault, parity error, address error
0	0	1	0	ARITHN	ALU arithmetic operation without carry
0	0	1	1	ARITHC	ALU arithmetic operation with carry
0	1	0	1	INCFPA	Increment file page address
0	1	0	0	INCTFA	Increment file address
0	1	1	0	SFTL2R	Shift L2 right; increment file address
0	1	1	1	SFTL2L	Shift L2 left; increment file address
F1 Field Strobes					
1	0	0	0	REQDMA	Set request DMA
1	0	0	1	CLRDMA	Clear DMA flag
1	0	1	0	RPLYAQ	Set A/Q reply
1	0	1	1	RJCTAQ	Set A/Q reject
1	1	0	0	STBCB1	Strobe selected control bits
1	1	0	1	CLRUDC	Clear up/down counter
1	1	1	0	SETDMA	Force set DMA flag
1	1	1	1	LDPNR	Load port number register form ALU output
F1 Field Bit Generator					
0	0	0	0	BG0	Select bit generator bit 0
0	0	0	1	BG1	Select bit generator bit 1
0	0	1	0	BG2	Select bit generator bit 2
0	0	1	1	BG3	Select bit generator bit 3
0	1	0	0	BG4	Select bit generator bit 4
0	1	0	1	BG5	Select bit generator bit 5
0	1	1	0	BG6	Select bit generator bit 6
0	1	1	1	BG7	Select bit generator bit 7

TABLE 4-10. F1 FIELD CONTROL (Contd)

F1 Field Bits				Mnemonic	Action
11	10	9	8		
F1 Field Auxiliary Conditions					
0	0	0	0	NSCHER	No stop on channel error jumper
0	0	0	1	T1PWAO	Type 1 PWAs only (HI) jumper
0	0	1	0	PRIT2	Primary PWA in type 2 (LO) jumper
0	0	1	1	EXTT2	External PWA is type 2 (LO) jumper
0	1	0	0	PPNOT	Not program protect
0	1	0	1	READ	A/Q read selected
0	1	1	0	L2BIT0	Latch 2 output bit zero (before shift, if shifting also)
0	1	1	1	L2BIT7	Latch 2 output bit seven (before shift, if shifting also)
1	0	0	0	DMAFLG	DMA flag, indicates DMA needs service
1	0	0	1	AQRDWT	A/Q flag, indicates A/Q read or write operation
1	0	1	0	SEGEQ3	Segment equal 3
1	0	1	1	DSRSET	DSR/DCD multiplexer set to DSR
1	1	0	0	TxRDY	Transmitter ready (needs data)
1	1	0	1	NOTERR	Not memory error (MPE, MPF, or MAE)
1	1	1	0	MPF	Memory protect fault
1	1	1	1	MAE	Memory Address error

TABLE 4-11. F2 FIELD CONTROL

F2 Field Bits				Mnemonic	Action
7	6	5	4		
F2 Field Enables					
0	0	0	0	LDFA1	Load file address register (F2/F3 bits to file address)
0	0	0	1	LDDMA	Load DMA address high bits
0	0	1	0	LDDTL	Load DMA data register lower
0	0	1	1	LDDTU	Load DMA data register upper
0	1	0	0	PEPNR	Enable priority encoder output to port number
0	1	0	1	INCTFA1	Increment file address
0	1	1	0	LDDMAL	Load DMA address register lower
0	1	1	1	LDDMAU	Load DMA address register upper

TABLE 4-11. F2 FIELD CONTROL (Contd)

F2 Field Bits				Mnemonic	Action
7	6	5	4		
F2 Field Strobes					
1	0	0	0	ROMPG0	Set ROM page 0 on next jump (JPT) or transform (XFM)
1	0	0	1	ROMPG1	Set ROM page 1 on next jump (JPT) or transform (XFM)
1	0	1	0	SETTM	Set test mode
1	0	1	1	PLDUDC	Load up/down counter (segment number) from field F3
1	1	0	0	LDPCR	Load port control register from field F3
1	1	0	1	CNTUP	Increment up/down counter (segment number) from field F3
1	1	1	0	CNTDWN	Decrement up/down counter (segment number)
1	1	1	1	RSTPEL	Reset priority encoder latch for next RxRDY
F2 Field Control Bits 1					
0	0	0	0	CLRRD	Clear DMA read
1	0	0	0	SETRD	Set DMA read
0	0	0	1	CLRPRT	Clear DMA protect
1	0	0	1	SETPRT	Set DMA protect
0	0	1	0	CLRDCD	Clear data carrier detected selector inputs
1	0	1	0	SELDSR	Select data set ready selector inputs
0	0	1	1	MAB201	If DMA-MAB20 equals 1
1	0	1	1	MAB200	If DMA-MAB20 equals 0
0	1	0	0	PRTDDS	Port data disable
1	1	0	0	PRTDEN	Port data enable
0	1	0	1	MAB181	If DMA-MAB18 equals 1
1	1	0	1	MAB180	If DMA-MAB18 equals 0
0	1	1	0	CLRBRG	Drop baud rate generator strobe
1	1	1	0	SETBRG	Set baud rate generator strobe
0	1	1	1	CLRINT	Clear program interrupt
1	1	1	1	SETINT	Set program interrupt

the instruction selector is inactive, the upper 512 instruction set is enabled. Selection of the multiplexer test inputs is determined by the firmware condition field (table 4-2). The selector has two hardwired inputs that provide the selection of unconditional instruction sequencing. The selector also provides for testing of the carry (ALUCY0) and comparison (AUEQFF) ALU outputs, the relative file address equal to all ones (FRAEQF), the common controller auxiliary conditions (auxiliary operation table 4-8), and the receiver ready (RxRDY) conditions.

Auxiliary Condition Selector

The common controller auxiliary condition selector comprises two eight-to-one multiplexers (U62 and U72) that are controlled by the firmware F1 field. These selectors provide for testing of an additional seven common conditions and four communication interface conditions (table 4-8). Five asynchronous signals are synchronized by a D-type latch before they are coupled to the selector inputs. Two inputs (DMAFLG and AQRDWT) are from the common controller; and three inputs (SEGEQ3, DSRSET, TxRDY) are from the communication interface. These signals are synchronized to the clock (TCLK) pulse by register U63. The no-stop-on-error jumper provides for selection of the no-stop-on-error bit.

S1 Field Decoder

The S1 field is partially decoded by a three-to-eight decoder (U32). This decoder controls the selection of general-purpose register L1, the data from memory register, the file data register and A/Q data upper, the file address register and A/Q data lower and PB-XI. Three bits (C24, C25, and C26) of the S1 field select the function, and the fourth S1 field bit (C23) selects the function input. (For example, C24 through C26 select data from memory, and the state of C23 selects the upper or lower data byte; C24 through C26 select file and upper A/Q data, and the state of C23 selects the file of the A/Q data.) After the function category selection has been made, the active and inactive condition of C23 and $\overline{C23}$ designate the functional operation. Refer to table 4-3. Since the enables are hardwired, the code (from the firmware S1 field) applied to the select inputs activates the associated output line.

Destination Field Decoder

The destination field is decoded by a three-to-eight line decoder (U30). This decodes the designation of the ALU output data, in accordance with the code (C14, C15, and C16) applied to the selected inputs. Refer to table 4-6.

F1 Field Decoders

The F1 field decoders consist of the bit generator (U71), F1 enables decoder (U51), and F1 strobes decoder (U40), which are all three-to-eight line decoders. The F1 enables and strobes selectors are enabled by the enables field (tables 4-7 and 4-8). The bit generator selects one of the output lines (BG0 through BG7) to go active (table 4-8) according to the code applied to the select inputs. The enables and strobes decoders are selected by the auxiliary E1 field bit C11A and activated by the F1 field bit C13. When C11 is low, the F1 strobes are enabled; and the F1 enables and the bit generator are disabled (table 4-8). The code applied to the select bits determines the selection, and C13 high-activates the F1 enables. The F1 strobes are synchronized by the clock pulse (TCLK). The F1 enables select control signals, and the F1 strobes select data transfers.

F2 Field Enables Decoder

The F2 field enables decoder is a three-to-eight line decoder (U52). The decoder selection is designated by bits C04 through C06 (table 4-9), enabled by bit C07, and activated by the E2 field bit C12.

F2 Field Control Bits

The F2 field control bits 1 register (U41) provides for selection of one of eight static signals (table 4-9). The register is connected as an eight-bit, addressable latch. The latch is addressed by the three least significant F2 field bits (C04 through C06). The most significant bit (C07) determines whether the latch should be set or cleared when the F1 strobe is applied. An active master clear ($\overline{MC}$) resets the register.

Direct Memory Access (DMA) Control

The direct memory access (DMA) control (figure 4-8) initiates, monitors, and controls the DMA data and address transfers programmed by the firmware. All data transfers between the communication interface and the central processor are DMA executed by the common controller DMA control logic. The direction of transfer is determined by the DMA WRITE signal, and program protection is provided by the DMA PROT signal. This control logic initiates a DMA request (DMA-MR) signal when the request DMA (REQDMA) signal from the F1 strobes selector becomes active and resets the DMA request latch U43. This request is accompanied by a DMA address. When the request signal is accepted by the DMA, it returns a request accepted (DMA-RA) signal and a data strobe signal (DMA-MDS). Thse signals are ANDed by gate U54. The resultant output clears the DMA-MR latch (U43), sets the DMA flag latch (U43), and activates the data from memory (STB-DFM).

If this is a read transfer when the STB-DFM goes high, the DMA data is loaded into the controller data from memory registers (U125 and U137).

The DMA request accepted (DMAX-RA) also enables the DMA error-detection logic and activates the enable address data (E-ADD-DATA) signal. If this is a write transfer, the E-ADD-DATA signal places the DMA address and data bits (residing in the DMA address and data registers) on the respective DMA-DTM and DMA-MAB busses.

The error-detection logic monitors the DMA memory parity error (DMA-MPE) and the DMA memory address error (DMA-MAE) lines from the DMA memory interface. If any line becomes active, the associated error latch (memory parity error U34 or address error U45) is set.

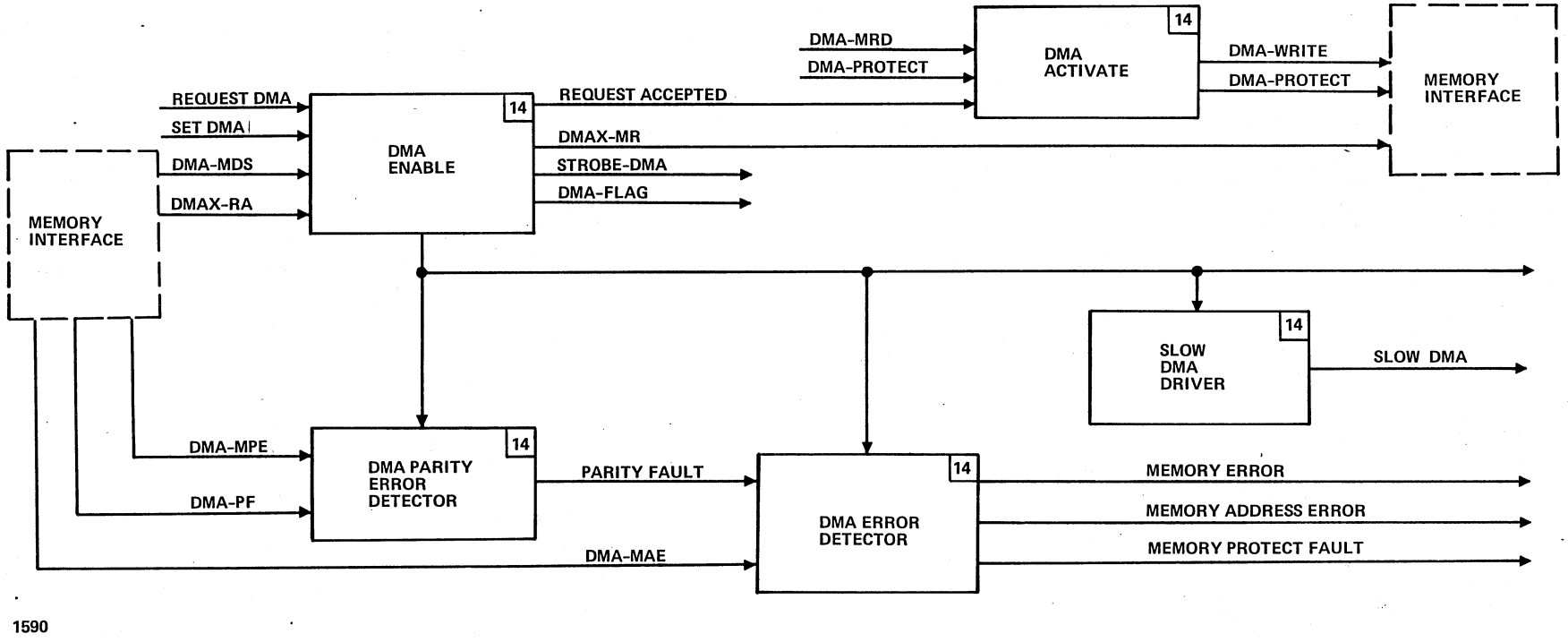


Figure 4-8. DMA Control

Either error activates the memory error (MEM-ERR) signal; and the firmware tests the conditions to determine which error occurred, address or parity. The error sets an associated status bit, and a clear error (CLRERR) resets the error latches at the next clock pulse (TCLK).

When the DMAFLG signal is sensed by the firmware scanner loop, the scanner loop checks the data direction and the full or empty condition of the DMA buffer in the file. If data can be transferred, DMAFLG is cleared by the clear DMA (CLRDMA) signal resetting latch U43. The DMA address in the file is udpated; if the DMA last word address has not been encountered, indicating that the DMA transfer is not complete, the DMA request (DMAX-MR) is set again.

The SLOW-DMA and DMA protect fault (DMA-PF) logic elements of the common controller are connected, but the circuits are not used. Since the BCLA is a protected device, these protect conditions are not required.

A/Q Control

The A/Q control (figure 4-9) detects, initiates, and controls function and status data transfers between the communication controller and the central processor via the I/O-TTY controller programmed by the firmware. In this mode of operation, data transfer is accomplished via the central processor A register in accordance with the Q-register commands. (Refer to I/O operations in section 2. The commands and the equipment designation are contained in the address line bits ADR01 through ADR16, (Q register bit 0 = ADR01). The upper eight address bits, ADR09 through ADR16, are used to select the equipment. The lower eight address bits designate the BCLA function/status command.

Control of the A/Q interface is a firmware task. The hardware consists of a latch (U65) that is set by the read and write signal from the SMI when the BCLA controller has been selected. The latch state is sensed by the firmware scanner. If the command can be executed, the firmware responds and sets the reply latch (U43). If the command cannot be executed, the reject latch (U43) is set. These latches are set by the F1 strobes selector. When either the reply or reject latch is set, the A/Q read/write latch is reset. The replay and reject latches are cleared by the absence of a read or write signal.

The data transfer between the central processor and the BCLA controller are conducted, via the I/O-TTY controller send lines SD01 through SD16 (A-register bit 0 = SD01) and read lines RD01 through RD16 (A-register bit 0 = RD01).

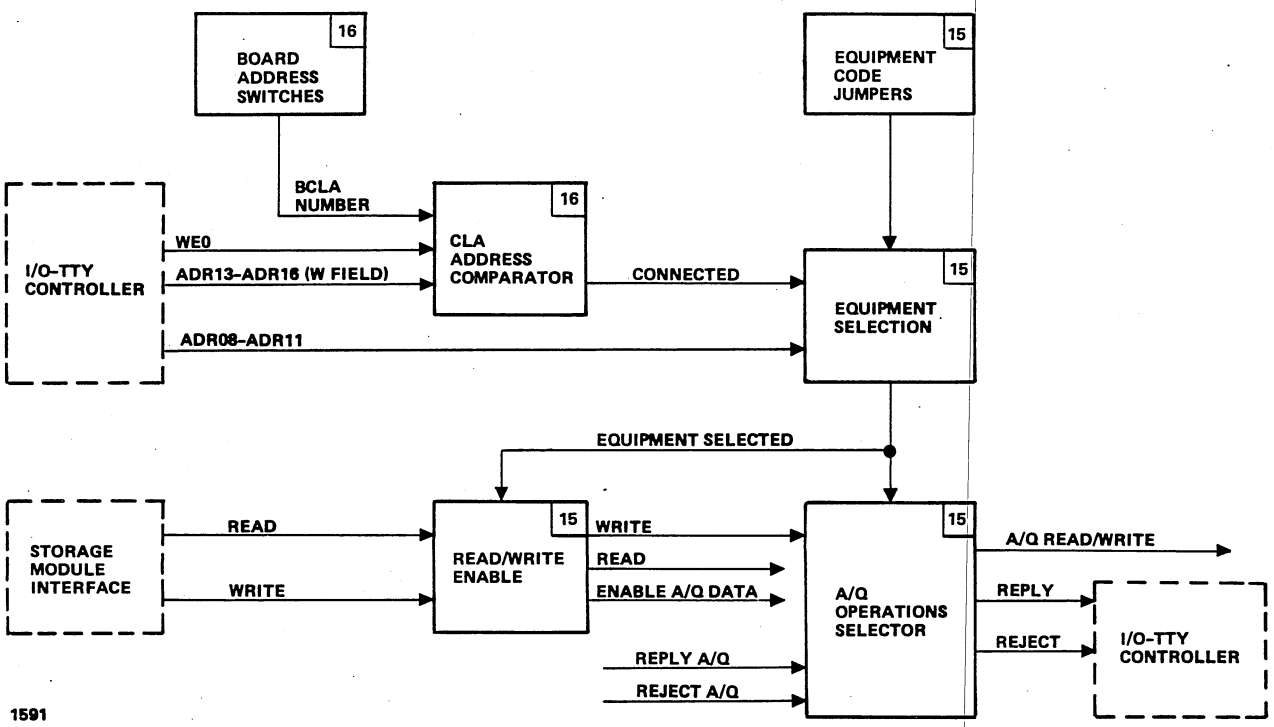


Figure 4-9. A/Q Control

COMMUNICATIONS INTERFACE

A BCLA subsystem provides six or sixteen asynchronous communication ports of RS232-C voltage interface data transfer. A sixteen-port communication subsystem consists of two printed wiring assemblies (PWAs) that are referred to as a primary BCLA and an expansion BCLA. The primary BCLA contains six communication ports, and the expansion BCLA contains ten communication ports. Each port provides two communication channels receive (read) and transmit (write) that can perform in full duplex mode (read and write simultaneously) or half duplex mode (read and write alternately). All communication ports are transparent to the processor.

Primary BCLA

The primary BCLA (figure 4-10) contains data transfer facilities for six communication ports and communication interface control facilities for control of sixteen communication ports.

Data Transfer

The data transfer facilities consist of six universal synchronous/asynchronous receiver/transmitter (USART) communication ports (00 through 05), three dual baud rate generators (one for every two ports), and test mode decoders. The data transfer facilities provide for read and write of data and status transfers between the processor, in which the BCLA subsystem is installed and the peripherals are attached to the ports.

Data is transferred by the communication interface to the terminal (write) when the write line is active, the port data latch enabled, and the baud rate code latch enabled. Then the eight bits of the first ALU byte contain the data that is loaded in to the USART transmit buffer. The next ALU byte upper four bits designate the baud rate. If a full duplex data transfer is in progress, the same baud rate is used for both receive and transmit serial data transfers.

USART

The USART provides the data and status communications between the attached terminal and processor via the common controller. It is programmed by the common controller firmware to transfer serial data to and from the terminal and parallel data to and from the common controller. The USART accepts (write) data characters from the common controllers, via the ALU bus, in parallel format and converts them into serial data for transmission. Simultaneously or alternately, it can receive serial data characters and convert them to parallel format for transfer to the common controller via the S1 bus. The USART signals the common controller whenever it can transfer a new character to or from the terminal. The parallel character may consist of five, six, seven, or eight bits, as determined by the port mode (see section 2). The USART adds (during writes) or deletes (during reads) the start, parity, and stop bits. The USART (figure 4-11) contains a data bus buffer, read/write control, modem control, transmit buffer, transmit control, receive buffer, and receive control logic.

The data bus buffer is a bidirectional eight-bit buffer used to interface with the BCLA port data bus. Data is transmitted or received by this buffer upon execution of a write or read instruction from the firmware F3 field. Control, command, and status characters are also transferred through the data bus buffer.

The read/write control logic detects the operational mode, strobe, and enable signals designated by the common controller. When reset is high, the USART is forced into the idle mode. It remains in idle mode until a new control word is applied. A reset must always precede a transfer mode change. A low on the write line ($\overline{WR}$) informs the USART that a control or data word is being loaded. A low on the read line ($\overline{RD}$) informs the USART that a data or status word is being sent to the common controller. The control/data (C/$\overline{D}$) input designates whether the write or read input is in control, status, or data word. When the line is high during a write cycle, the input is a control word; when it is high during a read cycle, the input is a status word. When the C/$\overline{D}$ line is low during either write or read mode, the character is a data word.

The chip select (CS) line activates the USART when a low state exists. When this line is high, the USART data bus is in the high-impedance state; and the mode select lines have no effect on the chip. The clock input generates internal USART timing, and no receive or transmit operations are referenced to this clock pulse. The receive and transmit timing is provided by the baud rate generator timing pulse applied to the transmit clock (TxC) and receive clock (RxC) inputs.

The modem control input and output data set ready (DSR), clear to send ($\overline{CTS}$), data terminal ready (DTR), and ready to send (RTS) are used to determine the status of the modem.

The transmit buffer accepts parallel data from the data bus buffer, inserts the designated parity and stop bits, and transmits a serial bit stream to the terminal (modem) via the transmit data (TxD) line. The transmission begins if clear to send (CTS) is active. The TxD line is held in the marking state if CTS is inactive, if the transmitter empty (TxEMPTY) is active, or if a reset applied.

The transmit control logic manages all activities associated with the transmission of serial data. It accepts both internal and external signals to accomplish this function. A transmitter ready (TxRDY) signal advises the common controller that the USART is ready to accept data. The TxRDY is used as an interrupt during polling to inform the common controller firmware that the port is available or requires service. This line (TxRDY) is automatically reset by the leading edge of the write signal when a data character is loaded. The transmitter empty (TxEMPTY) signal is not used. In asynchronous transmission mode, the baud rate is a fraction of the actual TxC frequency. The baud rate frequency is designated by the upper four ALU bits (ALU4 through ALU7) applied to the baud rate generator. The baud rate is designated by the port mode setup word (A-register bits 04 through 09).

The receive buffer accepts serial data, converts this data to parallel format, checks for character bits unique to the data transfer (see section 2) and inputs the data to the S1 bus via the USART data buffer. The serial data is applied to the receive data (RxD) input and clocked into the receive buffer on the rising edge of the receive clock (RxC).

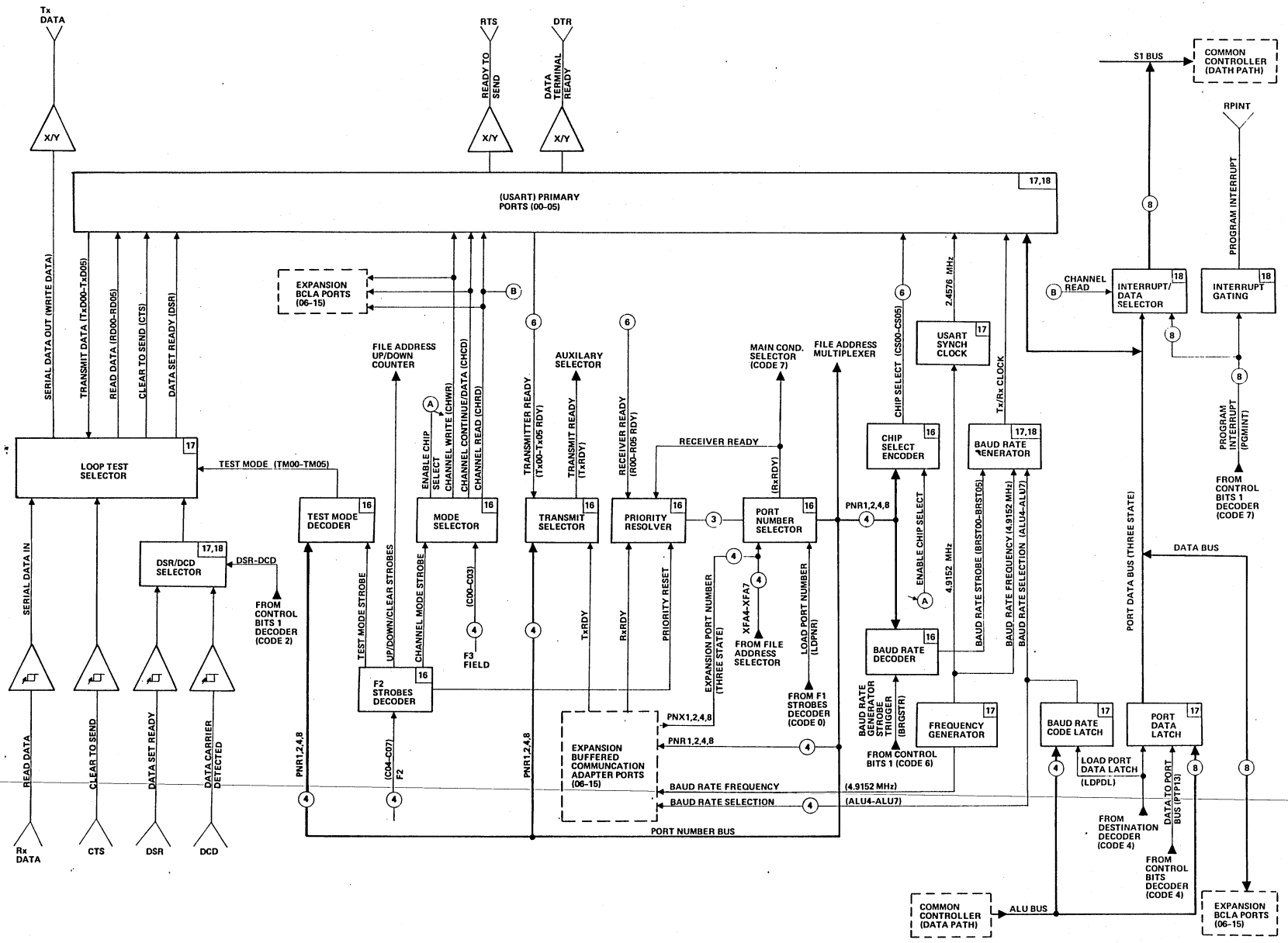


Figure 4-10. Primary BCLA Communication Interface Block Diagram

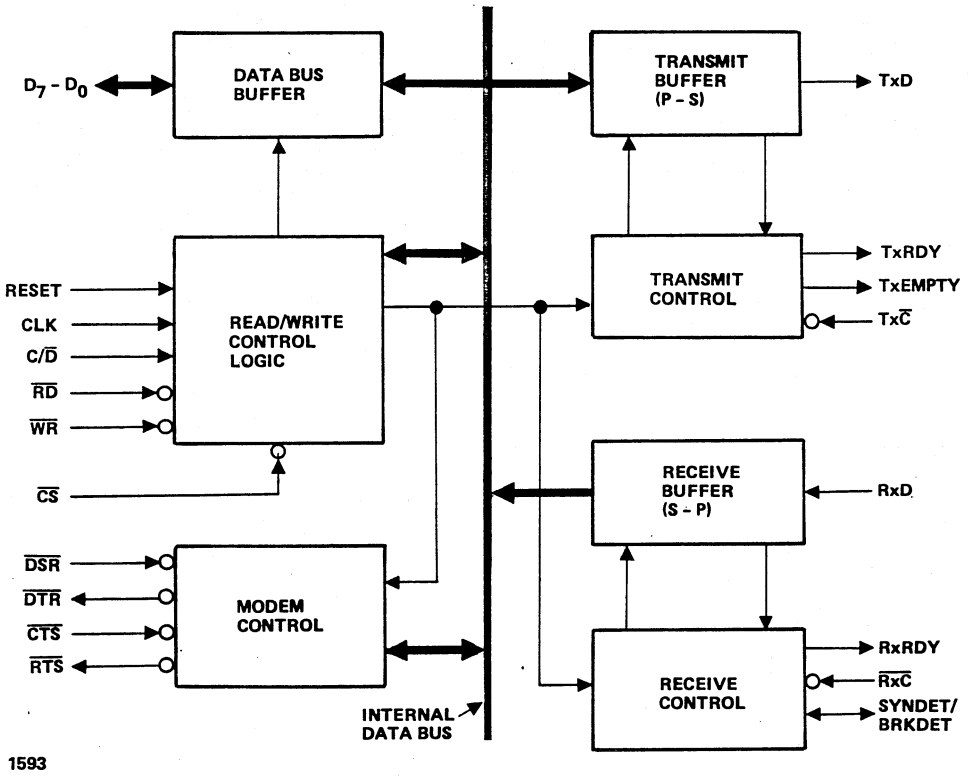


Figure 4-11. USART Block Diagram

The receive control logic manages all receiver-related activities of the USART. An initialization circuit prevents the USART from mistaking an unused input line for an active low data line in the break condition. Before starting to receive serial characters on the receive data (RxD) line, a valid high must first be detected after a chip master reset. Once this has been determined, a search for a valid low (start bit) is enabled. This search is done only once for each master reset. A false start detection circuit prevents false starts. Parity error detection circuits set the appropriate status bit when a parity error is detected. A framing error status is set if the stop bit is absent at the end of the character.

A receiver ready (RxRDY) output indicates that the receiver buffer contains a character that is ready for input to the processor. This sets an interrupt that is applied to the communication interface control priority encoder to advise the common controller that service is required. When the internal Rx enable is inactive, it masks and holds RxRDY in the reset condition. To set RxRDY in asynchronous mode, the receiver must be enabled to sense a start bit; and a complete character must be assembled and transferred to the receive data output register. Failure to read the received character from the receive data output register prior to assembly of the next character sets overrun status, and the previous character is written over and lost.

The receive clock (RxC) controls the rate at which the character is received. In asynchronous mode the baud rate (receive clock frequency) is a fraction of the actual clock frequency. The baud rate is the same for both transmit and receive operations in full duplex. The baud rate is designated by the ALU bits (ALU4 through ALU7) applied to the baud rate generator. The baud rate is designated by the port mode setup word (A-register bits 04 through 09).

Baud Rate

Baud rate is selected by the software A register data rate transfer field during a port mode setup command (see section 2). The baud rate decoder is enabled when the control bits 1 decoder code 6 is selected by the firmware (F2 field). After the decoder is enabled, the port number selector designates the port baud rate generator to be activated. All baud rate generators are coupled to a common frequency generator (baud rate oscillator) that produces a basic clock frequency of 4.9152 mHz. Each baud rate generator divides this basic clock frequency to produce 16 different, selectable baud rates (see section 2). The baud rate is selected by the ALU field and applied to the port designated by the port number selector. The port number is determined by the Q register bits Q3, Q4, Q5, and Q6 of the port mode command. The receive and transmit baud rates are the same for the individual port associated with a baud rate generator.

The baud rate latch (U94) applies the ALU field bits, ALU4 through ALU7 to all baud rate generators when the load port data latch (LPDL) is active. A latch in the baud rate generator loads the selection designated by the ALU field when the baud rate strobe is active. This selected baud rate is applied to the associated port USART until changed by the software.

The baud rate generators obtain the basic clock frequency from the baud rate oscillator (Y1). Output of the oscillator is coupled through AND gates (U23) and associated drivers (U8) to the respective baud rate generator. The AND gates allow for inhibiting the oscillator output and the insertion of a different basic clock frequency.

The baud rate decoder (U37) enables the loading of the ALU selection bits into the software-selected baud rate generator. The baud rate generator strobe, selected by the control bits 1 decoder code 6, enables all baud rate decoder outputs. The port number line (PNR1, 2, 4, and 8) designates the baud rate generator to load the ALU selection signal. Port number lines 1, 2, and 4 select one of the five strobe outputs (RST00 through RST05) when port number line 8 is low.

Test Mode

When test mode is selected, a loop test is initiated. The USART transmit data is coupled back to the USART receive data input to perform a loop test. The firmware enables the loop test mode decoder (U48), and the port number lines designate the test port. The test mode enable (TM00 through TM05) is active when the port number (PNR) 8 and test mode strobe are low at AND gate U13. This applies the active low to the strobe input of the loop test mode decoder. The active test mode signal sets the loop test selector to the loop test mode. This causes the USART transmit data output to be applied to the USART receive input, the clear to send input is forced active, and the normal clear-to-send signal is gated to the data set ready USART input. The data carrier detected and data set ready are irrelevant to loop test operation. When the test mode signal is inactive, the receive and transmit operations are independent. The data carrier detected and data set ready signals are polled by the control bits 1 decoder.

Control

All decoders and selectors of the primary BCLA control logic are eight element chips, but only six elements are used. When the port number line PNR8 is low, the primary BCLA control logic is active. When the port number line PNR8 is high, the expansion control logic is active. The F2 strobes decoder, port number selection, and mode selection logic for both the primary and expansion BCLA is located on the primary BCLA.

Port Number Select

The port number selector enables the port number lines (PNR1, 2, 4 and 8) consistent with the receive port priority or the firmware selection (file address XFA4 through XFA7).

During terminal communications the receive operations have highest priority, and the priority encoder provides the highest receive priority to the lowest number port. Transmit operations are processed in consecutive order by the firmware scanner routine (figure 4-12). The port number selector consists of a two-to-one multiplexer (U68) and latch (U80). When the priority encoder-port number (PE-PNR) is active and a port 00 through 05 port receiver requires service, the selector couples the active port code number to the port number selector latch. The port number then activates the control logic, baud rate decoder, and chip select encoder to select the port associated with the service request. The port number is also sent to the file address page selector to designate the file location. When a transmit operation is selected by the firmware, the port number code is designated by the file address bits (XFA4 through XFA7). The port number code is then coupled to the transmit selector, the test mode decoder, and the file page address selector. The file page address designates the file location of the data. When the associate port USART buffer is loaded, the write mode becomes active. If a loop test is requested, the firmware enables the test mode strobe.

Chip Select

The chip select encoder (U26) enables the USART associated with the port number selection when the chip select line is active.

Baud Rate Decoder

The baud rate decoder enables the associated port baud rate generator coincident with the port number selection.

Transmit Selector

The transmit selector (U59) enables the USART designated by the port number when PNR8 is low. When PNR8 is high, the selected USART is inhibited.

Mode Selector

The mode selector (U12) designates the operational mode of the active port. These modes are determined from the firmware F3 field bits (C00 through C03). The bit conditions enable the chip selection, control or data word selection, and write mode and read mode operations of the ports in the primary and expansion BCLA. These conditions are selected by the firmware F2 field (C04 through C07) code applied to the F2 strobes decoder. The mode selector is strobed by the trailing edge of code 4 select pulse (load port control register, LDPCR). F3 field bit C00 enables tht chip select decoders. Bit C01 designates that the character in the selected USART buffer is a control byte or a data byte (control = $\overline{\text{CHED}}$ high, data = $\overline{\text{CHCD}}$ low). Bit C02 selects the read mode, and bit C03 selects the write mode.

Firmware F2 Field Strobes Decoder

This decoder (U4) selects the strobes that activate the file address up/down counter, reset the priority encoders, load the mode selector, enable the test mode decoder, and select the firmware pages. These selections are designated by the F2 field bits C04 through C06, enabled by C07 and C12, and strobed by $\overline{\text{A-TCLK}}$. When C07 is high and the F2 enables bit C12 is high, the code produced by bits C04 through C06 is applied to the output at the low state of A-TCLK. Code selections 5 and 6 direct the up and down count operations of the up/down counter. When code 3 is active, the up/down counter is loaded to the preset count designated by the F3 field.

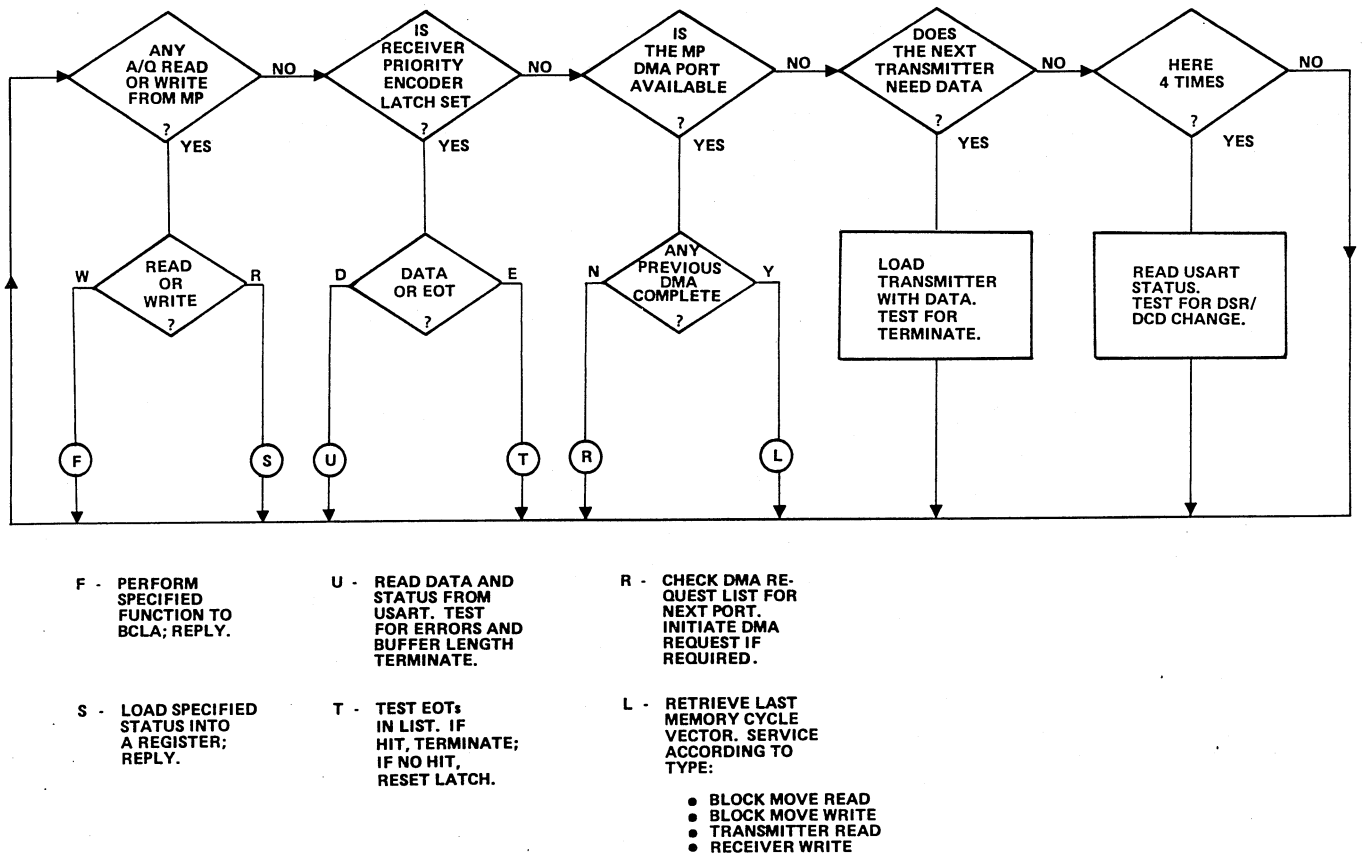


Figure 4-12. BCLA Firmware Scanner Routine

Test Mode Decoder

The test mode decoder (U48) selects the loop test operation of the port designated by the port number line (PNR1, 2, 4, and 8) conditions. When the F2 strobes decoder selects test mode, port number line 8 designates the primary BCLA when low and expansion BCLA when high. The code produced by port number lines 1, 2, and 4 designates the active port. This selected port output (TM00 through TM05) enables the loop test mode to be selected by the associated loop test selector. During loop test no data is transmitted. The transmit serial data is coupled through the selector back to the USART receive serial data input.

Priority Encoder

The priority encoder is applicable only to the receive mode and consists of latch U78, inverters U92, and priority encoder U109. The encoder provides highest priority to the lowest numbered port. When one or more port receive ready line are active at the latch (U78) input, the A-TCLK strobe trailing edge latches the conditions. The priority encoder accepts inputs from eight active lines (low) and provides a corresponding binary code output. A priority is assigned to each input so that when one or more inputs are simultaneously active the input on line 7 (pin 4) has the higest priority. Therefore, if line 7 (R00RDY) is active, the encoder output lines are all low; and the port number selector enables all control and data elements associated with port 00. At this time the receive ready (RxRDY signal inhibits the clock strobe until the encoding is complete.

When input line 1 or 0 is active, the code 6 output is active. This produces a low output from AND gate U79. The port number selector (U68) is enabled to select priority inputs from the expansion BCLA.

Expansion BCLA

The expansion BCLA (figure 4-13) contains data transfer and control facilities for ten communication ports. The expansion data transfer and control logic function in the same manner as they do with the primary BCLA. These data transfer ports are transparent to the processor, and control and data are obtained from the primary BCLA. The baud rate and USART sync clock obtain basic frequency (4.9152 MHz) from the primary BCLA frequency generator.

Current Loop Adapter

The current loop adapter provides an isolated means of converting RS232-C voltage interface signals to current loop (20 mA) signals. During write operations the character bit conditions are converted from RS232-C digital signals to current loop digital signals. During read operations the current loop digital signals are converted to RS232-C digital signals.

The current loop adapter (figure 4-14) employs optical isolators that transfer the digital data from the voltage to the current interface. The optical isolator converter consists of an LED and photoelectic transistor. The on and off states of the LED are detected by the phototransistor and converted to voltage changes or current flow changes depending upon the direction of data flow.

During read operations the presence and absence of current flow from J3 pin 3 to the 24 V dc power supply cause the LED to illuminate or remain dark. These conditions are sensed by the phototransistor, which enables and disables the level converter conduction. The changes in voltage levels -9V to +9V applied to the drive are converted to 0 and 1 logic states. A zero state is designated by a voltage level less than +0.4V, and a 1 is designated a voltage level greater than 2.5V.

During a write operation the digital voltage states applied to the digital-to-light converter cause the LED to illumininate or remain dark. These changes in brightness of the LED are sensed by the phototransistor. The phototransistor turns the current switch on and off to create changes in current flow from J3 pin 2 to the 24 V dc power supply.

The 24 V dc power supply provides the current loop voltage source and the current loop adapter operational voltages.

The current loop adapters contain terminals that can be jumpered to select half duplex and full duplex operations (table 4-12). Jumpers may be inserted in the channel 2 terminals to enable an RS232-C voltage interface (table 4-12). The RS232-C voltage interface selection of channel 2 provides for system application of an odd or even number of current loop channels.

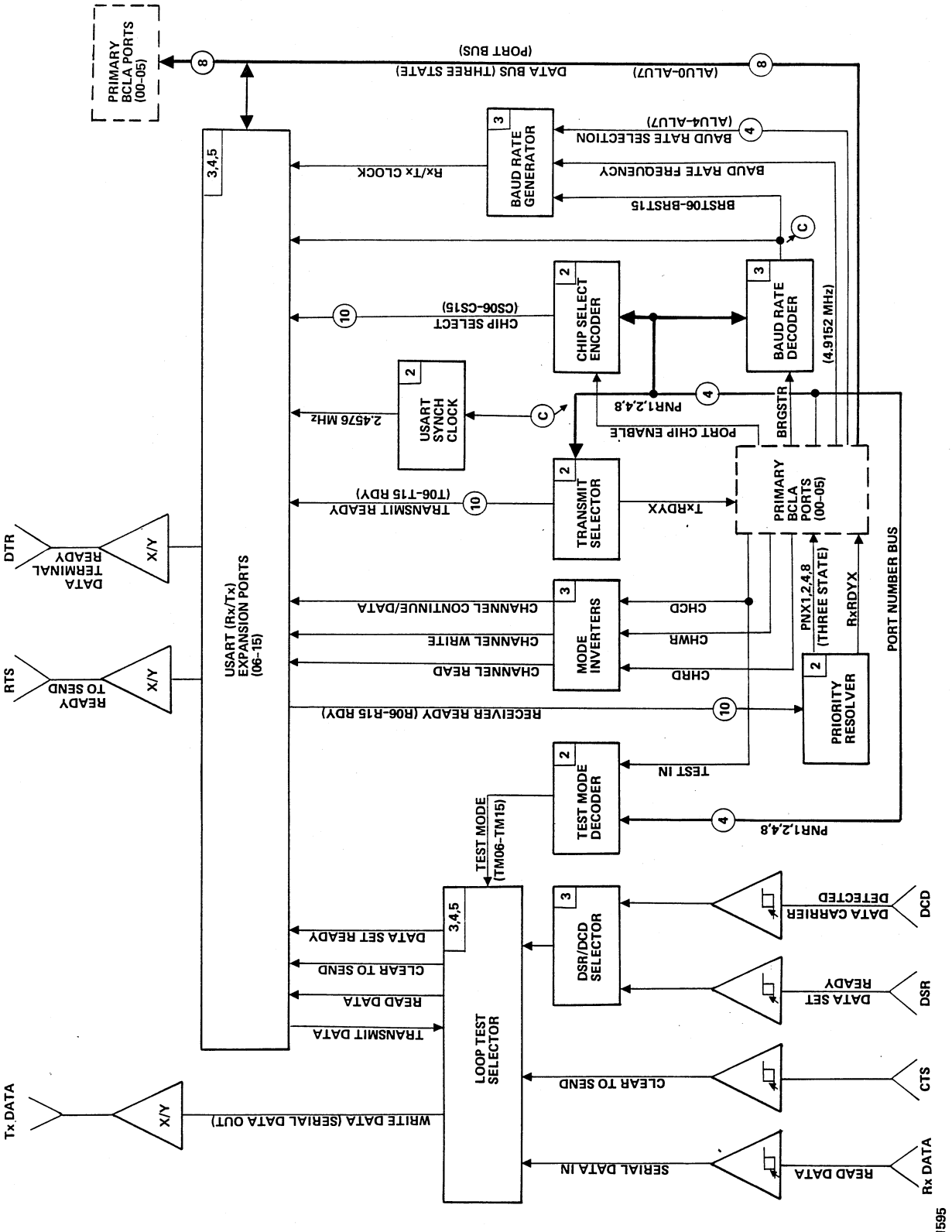


Figure 4-13. Expansion BCLA Block Diagram

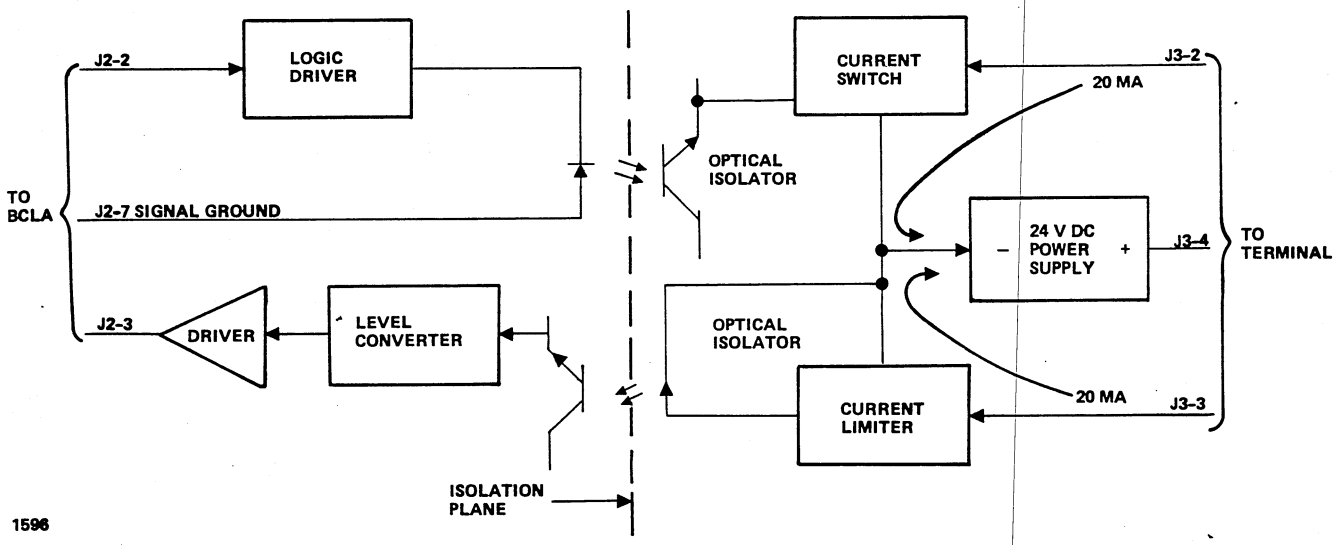


Figure 4-14. Current Loop Adapter Block Diagram

TABLE 4-12. CURRENT LOOP ADAPTER JUMPER SELECTION

Mode / Jumper	Channel 1 or 2 Full Duplex With Passive Receiver	Channel 1 or 2 Full Duplex (Keyboard Display or Console Display)†	Channel 1 or 2 Half Duplex (Keyboard Display) (CC555)	Channel 1 or 2 Half Duplex (Console Display)†† (CC6144)	Channel 2 Voltage Mode
Channel 1					
E1 to E2	In	In	Out	In	
E3 to E4	Out	Out	In	Out	
E5 to E6	In	In	Out	Out	Full or Half Duplex Jumpers
E15 to E14	Out	In	In	In	
E9 to E10	Out	Out	In	In	
E13 to E11	Out	In	Out	Out	
E8 to E7	In	In	In	In	In
E12 to E16	In	In	In	In	In

†= Code switches on console display set to 10010100
††= Code switches on console display set to 10100110

TABLE 4-12. CURRENT LOOP ADAPTER JUMPER SELECTION (Contd)

Mode / Jumper	Channel 1 or 2 Full Duplex With Passive Receiver	Channel 1 or 2 Full Duplex (Keyboard Display or Console Display)†	Channel 1 or 2 Half Duplex (Keyboard Display) (CC555)	Channel 1 or 2 Half Duplex (Console Display)†† (CC6144)	Channel 2 Voltage Mode
Channel 2					
E52 to E53	In	In	Out	In	X
E49 to E50	Out	Out	In	Out	X
E31 to E27	In	In	Out	Out	X
E26 to E30	Out	In	In	In	X
E32 to E28	Out	Out	In	In	X
E41 to E38	Out	In	Out	Out	X
E33 to E25	In	In	In	In	In
E20 to E21	In	In	In	In	In
E34 to E35	In	In	In	In	Out
E47 to E46	In	In	In	In	Out
E55 to E56	In	In	In	In	Out
E18 to E19	In	In	In	In	Out
E43 to E40	In	In	In	In	Out
E42 to E39	In	In	In	In	Out
E22 to E23	In	In	In	In	Out
E59 to E60	Out	Out	Out	Out	In
E29 to E54	Out	Out	Out	Out	In
E48 to E36	Out	Out	Out	Out	In
E17 to E24	Out	Out	Out	Out	In
E51 to E37	Out	Out	Out	Out	In

X = Don't care
† = Code switches on console display set to 10010100
†† = Code switches on console display set to 10100110

DIAGRAMS 5

This section contains the logic diagrams for the primary and expansion printed wiring assemblies of the buffered communication line adapters and schematic diagrams applicable to associated assemblies.

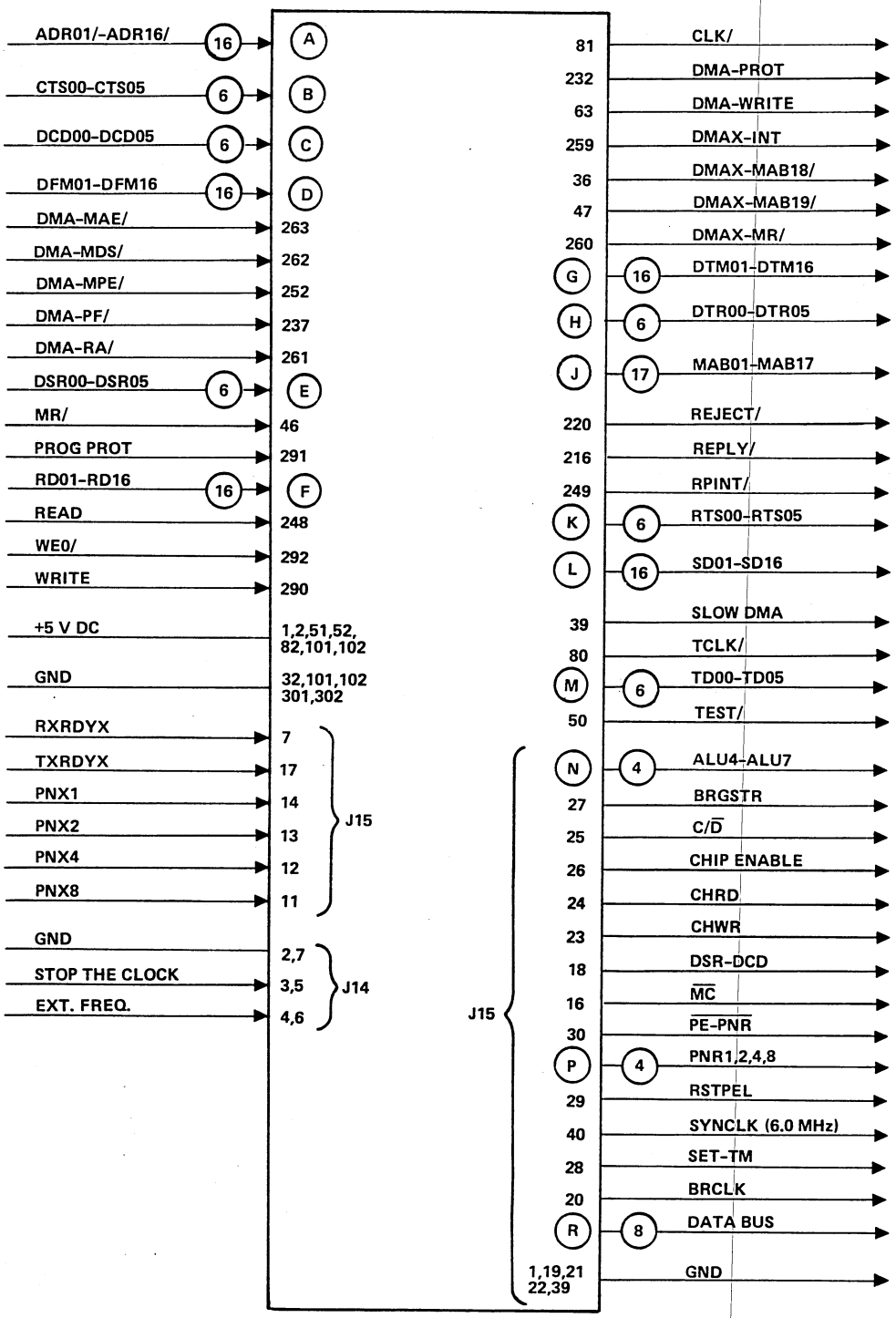


Figure 5-1. Primary BCLA External Data and Control Signals (Sheet 1 of 3)

(A)

ADR01/-ADR16/	
ADR01	280
ADR02	247
ADR03	246
ADR04	245
ADR05	212
ADR06	217
ADR07	222
ADR08	281
ADR09	282
ADR10	283
ADR11	284
ADR12	285
ADR13	286
ADR14	287
ADR15	288
ADR16	289

(B)

CTS00-CTS05	
CTS00	6
CTS01	11
CTS02	16
CTS03	22
CTS04	27
CTS05	33

(C)

DCD00-DCD05	
DCD00	5
DCD01	10
DCD02	15
DCD03	20
DCD04	26
DCD05	31

(D)

DFM01-DFM16	
DFM01	264
DFM02	265
DFM03	266
DFM04	267
DFM05	268
DFM06	269
DFM07	270
DFM08	271
DFM09	272
DFM10	273
DFM11	274
DFM12	275
DFM13	276
DFM14	277
DFM15	278
DFM16	279

(E)

DSR00-DSR05	
DSR00	3
DSR01	8
DSR02	13
DSR03	18
DSR04	24
DSR05	29

(F)

RD01-RD16	
RD01	204
RD02	206
RD03	208
RD04	210
RD05	214
RD06	218
RD07	221
RD08	224
RD09	226
RD10	229
RD11	231
RD12	234
RD13	236
RD14	239
RD15	241
RD16	244

(G)

DTM01-DTM16	
DTM01	64
DTM02	65
DTM03	66
DTM04	67
DTM05	68
DTM06	69
DTM07	70
DTM08	71
DTM09	72
DTM10	73
DTM11	74
DTM12	75
DTM13	76
DTM14	77
DTM15	78
DTM16	79

(H)

DTR00-DTR05	
DTR00	4
DTR01	9
DTR02	14
DTR03	19
DTR04	25
DTR05	30

(J)

MAB01-MAB17	
MAB01	53
MAB02	54
MAB03	55
MAB04	56
MAB05	57
MAB06	58
MAB07	59
MAB08	60
MAB09	61
MAB10	62
MAB11	253
MAB12	254
MAB13	255
MAB14	256
MAB15	257
MAB16	258
MAB17	35

1597B

Figure 5-1. Primary BCLA External Data and Control Signals (Sheet 2 of 3)

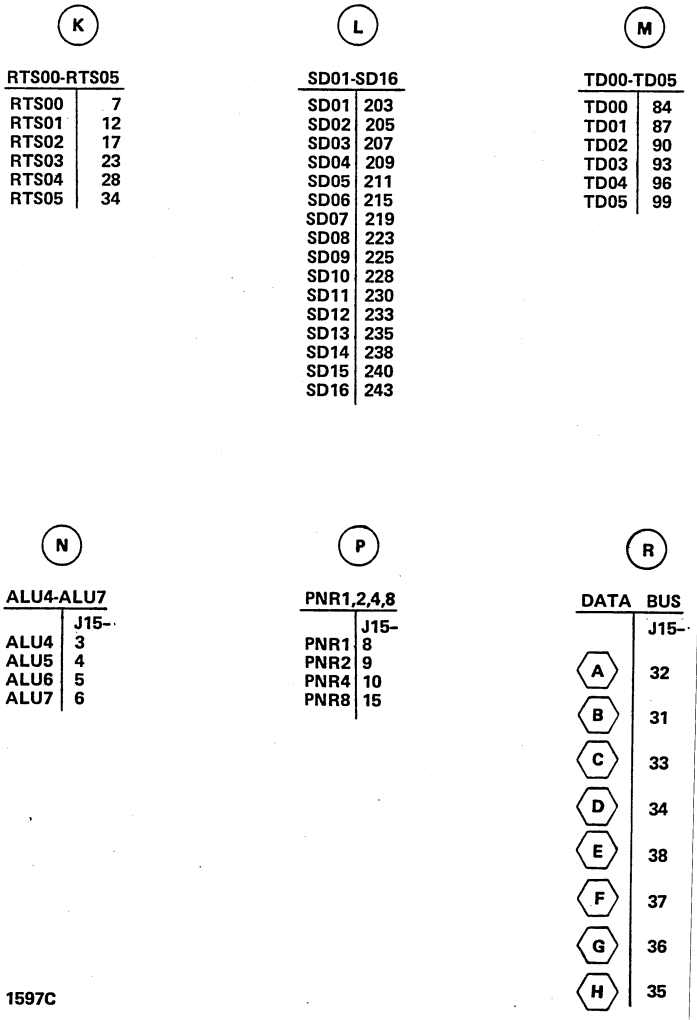
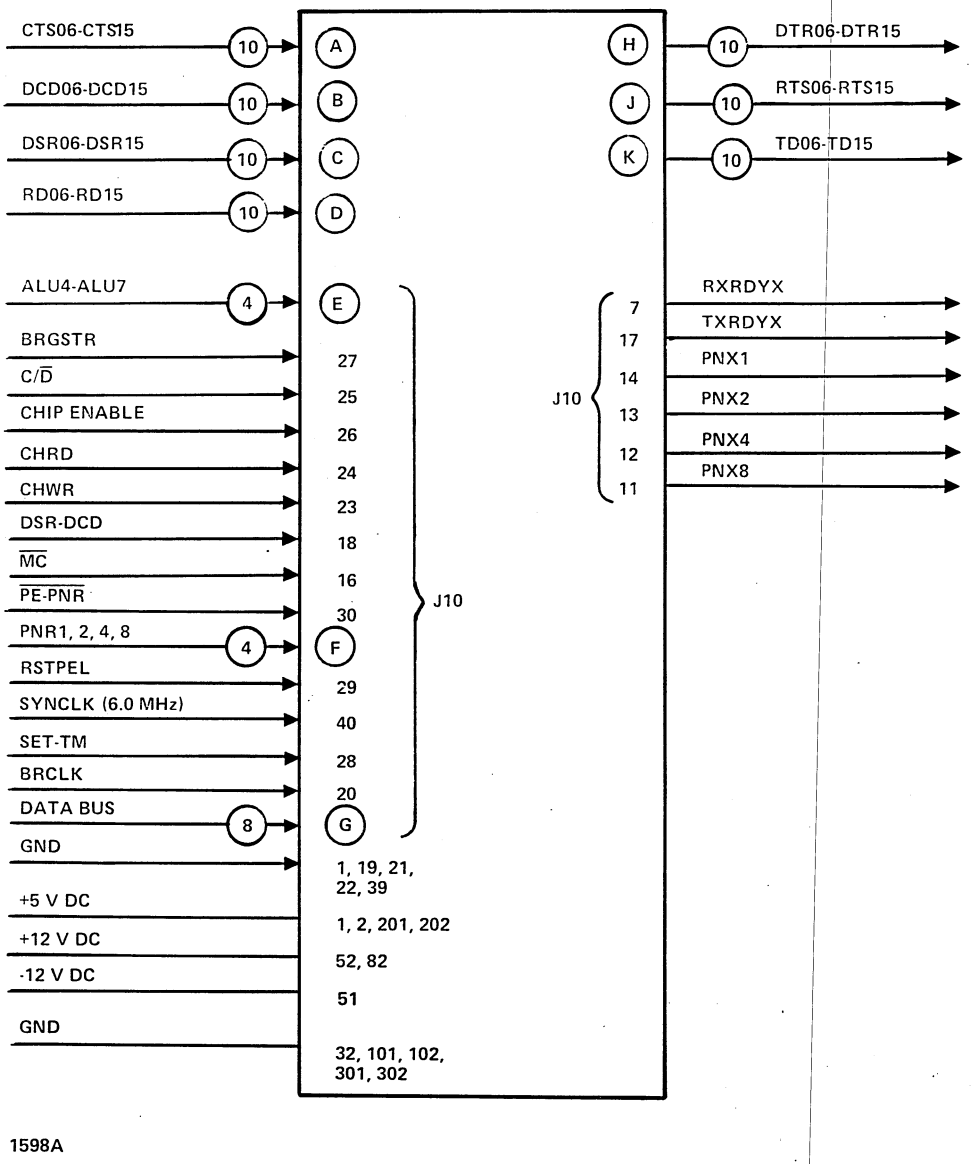


Figure 5-1. Primary BCLA External Data and Control Signals (Sheet 3 of 3)



1598A

Figure 5-2. Expansion BCLA External Data and Control Signals (Sheet 1 of 2)

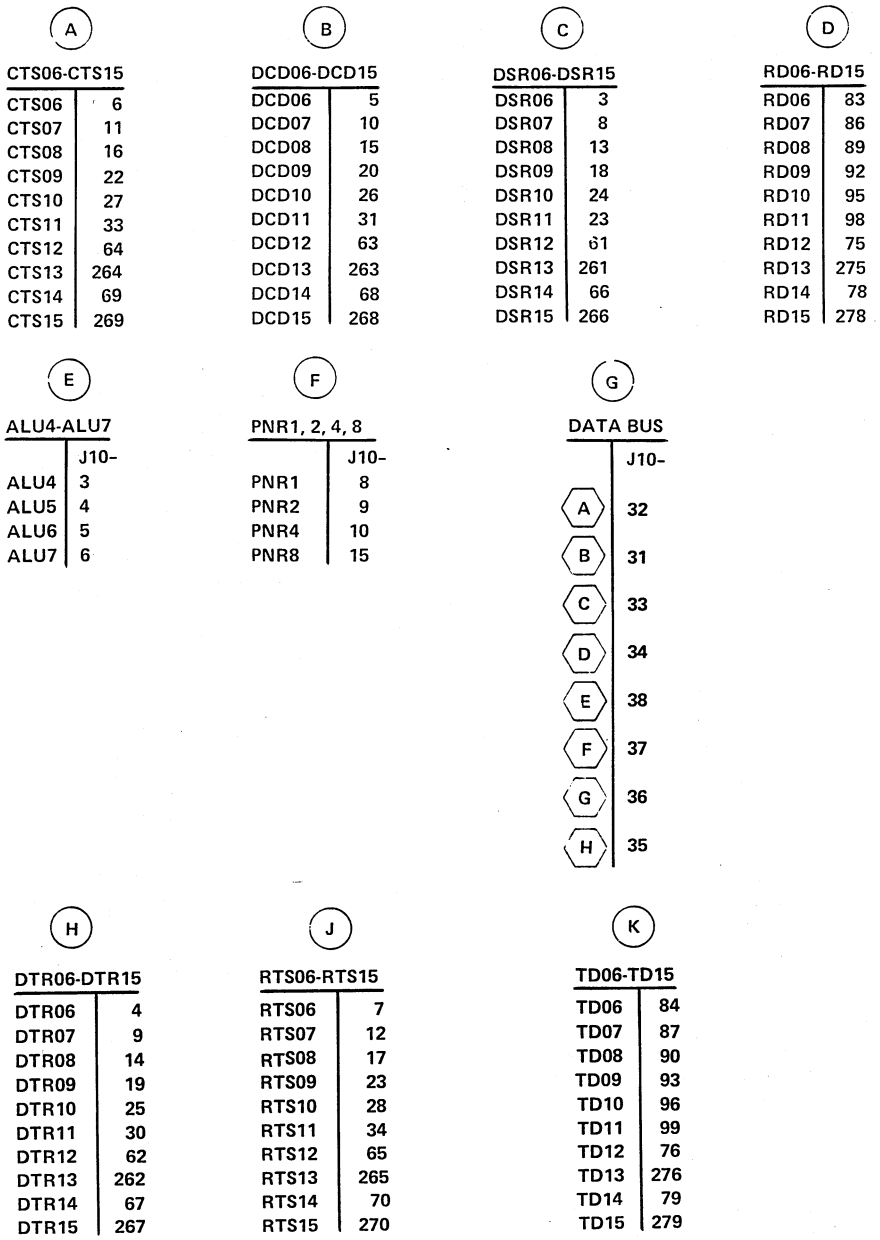
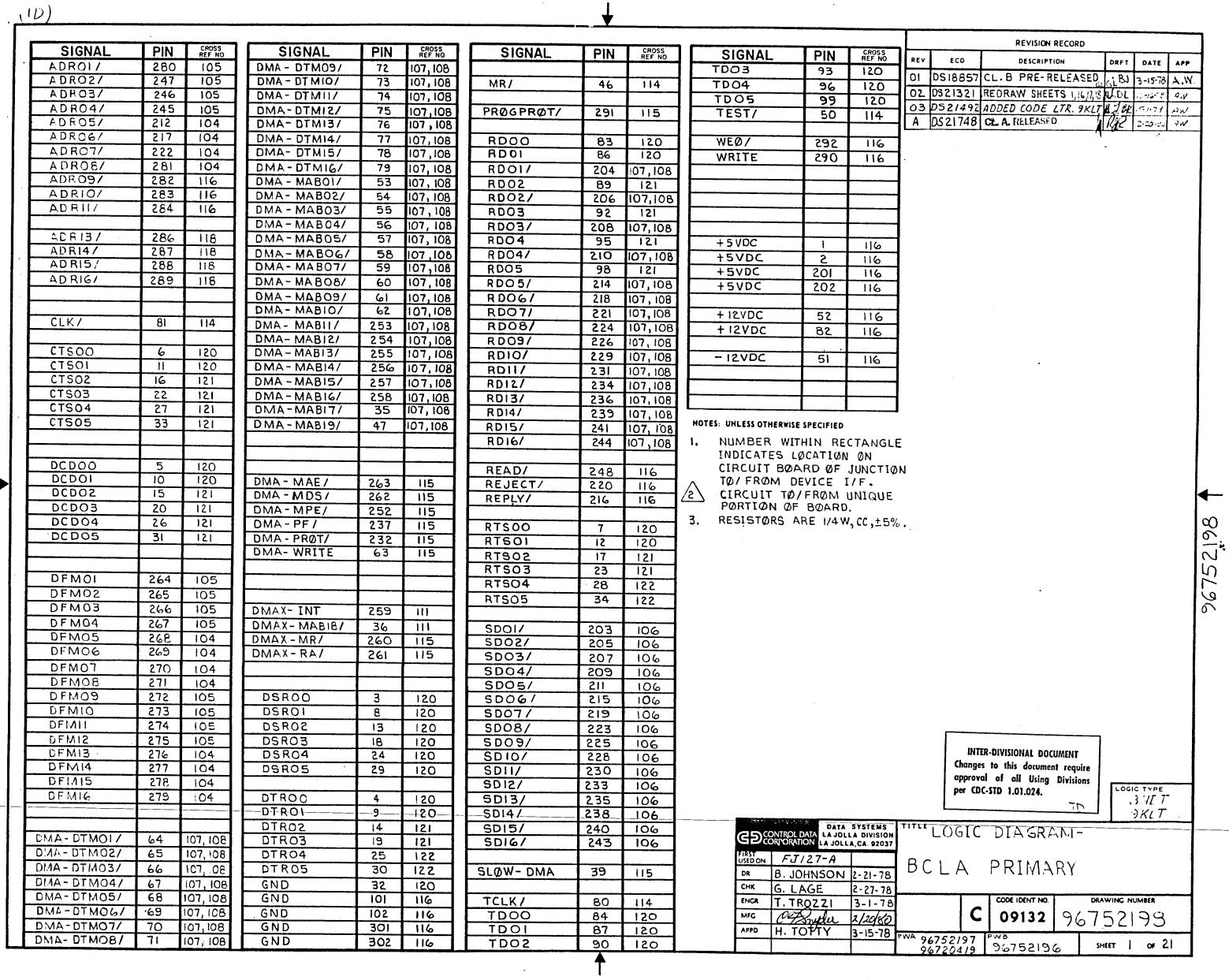


Figure 5-2. Expansion BCLA External Data and Control Signals (Sheet 2 of 2)



SIGNAL	PIN	CROSS REF NO
ADRO1/	280	105
ADRO2/	247	105
ADRO3/	246	105
ADRO4/	245	105
ADRO5/	212	104
ADRO6/	217	104
ADRO7/	222	104
ADRO8/	281	104
ADRO9/	282	116
ADRIO/	283	116
ADRII/	284	116
ADRI3/	286	118
ADRI4/	287	118
ADRI5/	288	118
ADRI6/	289	116
CLK/	81	114
CTSOO	6	120
CTSO1	11	120
CTSO2	16	121
CTSO3	22	121
CTSO4	27	121
CTSO5	33	121
DCDOO	5	120
DCDO1	10	120
DCDO2	15	121
DCDO3	20	121
DCDO4	26	121
DCDO5	31	121
DFMO1	264	105
DFMO2	265	105
DFMO3	266	105
DFMO4	267	105
DFMO5	268	104
DFMO6	269	104
DFMO7	270	104
DFMO8	271	104
DFMO9	272	105
DFMIO	273	105
DFMII	274	105
DFMI2	275	105
DFMI3	276	104
DFMI4	277	104
DFMI5	278	104
DFMI6	279	104
DMA-DTMO1/	64	107, 108
DMA-DTMO2/	65	107, 108
DMA-DTMO3/	66	107, 08
DMA-DTMO4/	67	107, 108
DMA-DTMO5/	68	107, 108
DMA-DTMO6/	69	107, 108
DMA-DTMO7/	70	107, 108
DMA-DTMO8/	71	107, 108

SIGNAL	PIN	CROSS REF NO
DMA-DTMO9/	72	107, 108
DMA-DTMIO/	73	107, 108
DMA-DTMII/	74	107, 108
DMA-DTMI2/	75	107, 108
DMA-DTMI3/	76	107, 108
DMA-DTMI4/	77	107, 108
DMA-DTMI5/	78	107, 108
DMA-DTMI6/	79	107, 108
DMA-MABO1/	53	107, 108
DMA-MABO2/	54	107, 108
DMA-MABO3/	55	107, 108
DMA-MABO4/	56	107, 108
DMA-MABO5/	57	107, 108
DMA-MABO6/	58	107, 108
DMA-MABO7/	59	107, 108
DMA-MABO8/	60	107, 108
DMA-MABO9/	61	107, 108
DMA-MABIO/	62	107, 108
DMA-MABII/	253	107, 108
DMA-MABI2/	254	107, 108
DMA-MABI3/	255	107, 108
DMA-MABI4/	256	107, 108
DMA-MABI5/	257	107, 108
DMA-MABI6/	258	107, 108
DMA-MABI7/	35	107, 108
DMA-MABI9/	47	107, 108
DMA-MAE/	263	115
DMA-MDS/	262	115
DMA-MPE/	252	115
DMA-PF/	237	115
DMA-PRØT/	232	115
DMA-WRITE	63	115
DMAX-INT	259	111
DMAX-MABI8/	36	111
DMAX-MR/	260	115
DMAX-RA/	261	115
DSROO	3	120
DSRO1	8	120
DSRO2	13	120
DSRO3	18	120
DSRO4	24	120
DSRO5	29	120
DTROO	4	120
DTRO1	9	120
DTRO2	14	121
DTRO3	19	121
DTRO4	25	122
DTRO5	30	122
GND	32	120
GND	101	116
GND	102	116
GND	301	116
GND	302	116

SIGNAL	PIN	CROSS REF NO
MR/	46	114
PRØGPRØT/	291	115
RDOO	83	120
RDO1	86	120
RDO1/	204	107, 108
RDO2	89	121
RDO2/	206	107, 108
RDO3	92	121
RDO3/	208	107, 108
RDO4	95	121
RDO4/	210	107, 108
RDO5	98	121
RDO5/	214	107, 108
RDO6/	218	107, 108
RDO7/	221	107, 108
RDO8/	224	107, 108
RDO9/	226	107, 108
RDIO/	229	107, 108
RDII/	231	107, 108
RDI2/	234	107, 108
RDI3/	236	107, 108
RDI4/	239	107, 108
RDI5/	241	107, 108
RDI6/	244	107, 108
READ/	248	116
REJECT/	220	116
REPLY/	216	116
RTSOO	7	120
RTSO1	12	120
RTSO2	17	121
RTSO3	23	121
RTSO4	28	122
RTSO5	34	122
SDO1/	203	106
SDO2/	205	106
SDO3/	207	106
SDO4/	209	106
SDO5/	211	106
SDO6/	215	106
SDO7/	219	106
SDO8/	223	106
SDO9/	225	106
SDIO/	228	106
SDII/	230	106
SDI2/	233	106
SDI3/	235	106
SDI4/	238	106
SDI5/	240	106
SDI6/	243	106
SLØW-DMA	39	115
TCLK/	80	114
TDOO	84	120
TDO1	87	120
TDO2	90	120

SIGNAL	PIN	CROSS REF NO
TDO3	93	120
TDO4	96	120
TDO5	99	120
TEST/	50	114
WEØ/	292	116
WRITE	290	116
+5VDC	1	116
+5VDC	2	116
+5VDC	201	116
+5VDC	202	116
+12VDC	52	116
+12VDC	82	116
-12VDC	51	116

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	DS18857	CL. B PRE-RELEASED	BJ	3-15-78	A.W
02	DS21321	REDRAW SHEETS 1,16,17,18	DL		A.W
03	DS21492	ADDED CODE LTR. 9KLT			A.W
A	DS21748	CL. A. RELEASED			A.W

NOTES: UNLESS OTHERWISE SPECIFIED

1. NUMBER WITHIN RECTANGLE INDICATES LØCATIØN ØN CIRCUIT BØARD ØF JUNCTIØN TØ/FRØM DEVICE I/F.
2. CIRCUIT TØ/FRØM UNIQUE PØRTIØN ØF BØARD.
3. RESISTØRS ARE 1/4W, CC, ±5%.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

LOGIC TYPE .3 MT 9KLT

CONTROL DATA CORPORATION — DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037

FIRST USED ON	FJ127-A	
DR	B. JOHNSON	2-21-78
CHK	G. LAGE	2-27-78
ENGR	T. TROZZI	3-1-78
MFG		2/29/80
APPD	H. TOPTY	3-15-78

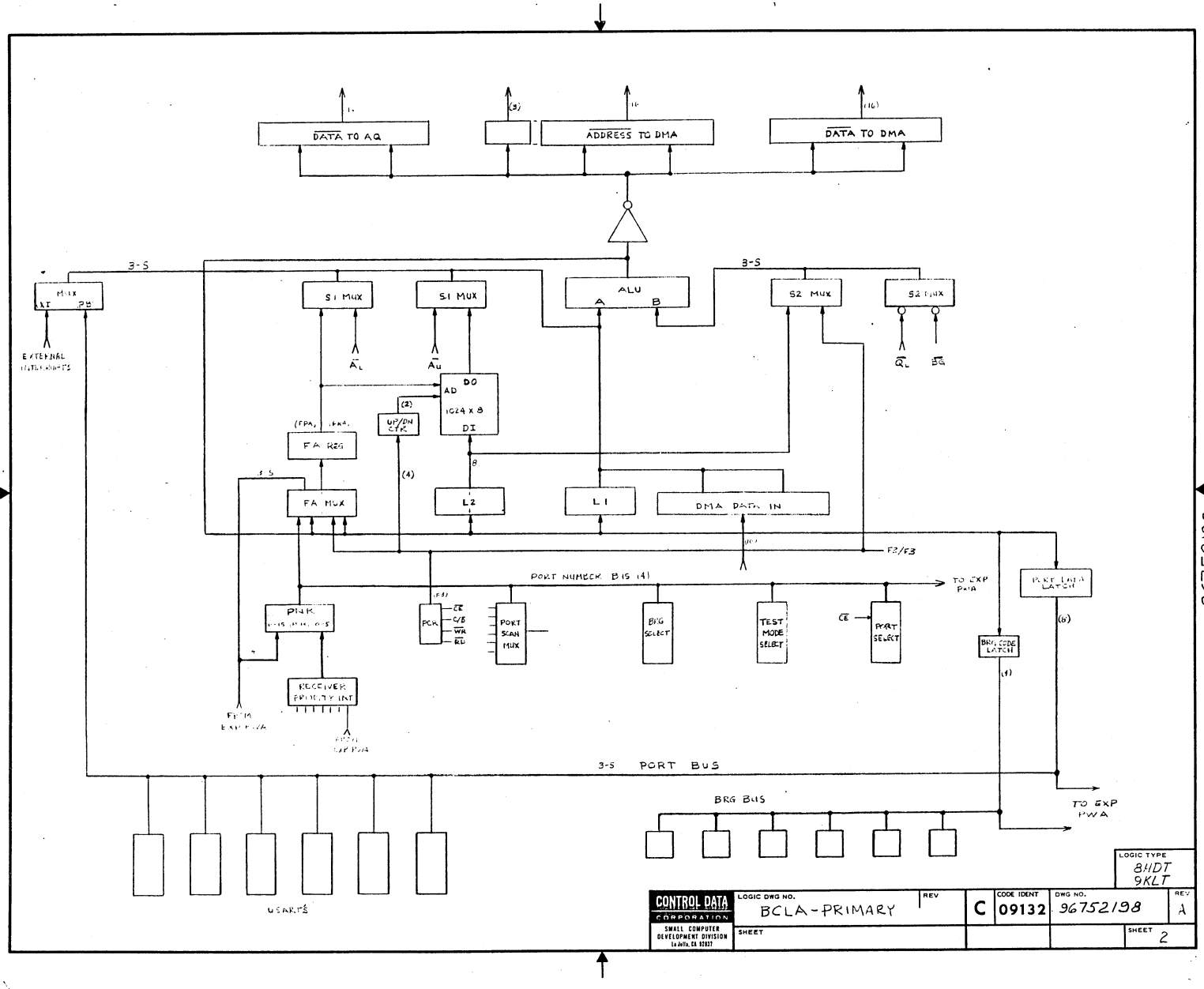
TITLE LOGIC DIAGRAM-
BCLA PRIMARY

C | CODE IDENT NO. 09132 | DRAWING NUMBER 96752193

PWA 96752197 96720419 | PWB 96752196 | SHEET 1 OF 21

96752198

Figure 5-3. Primary BCLA Logic Diagram (Sheet 1 of 21)



96752198

Figure 5-3. Primary BCLA Logic Diagram (Sheet 2 of 21)

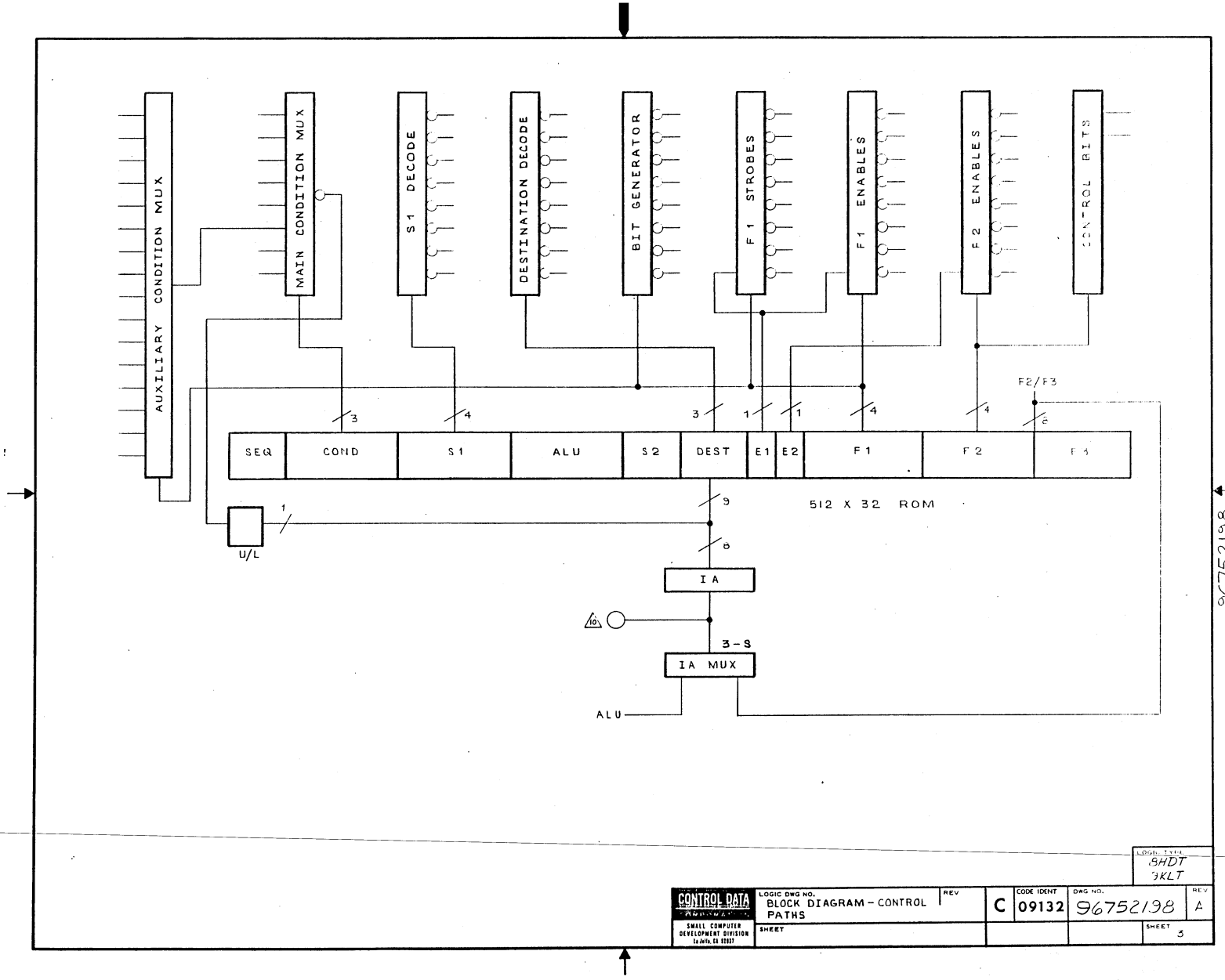


Figure 5-3. Primary BCLA Logic Diagram (Sheet 3 of 21)

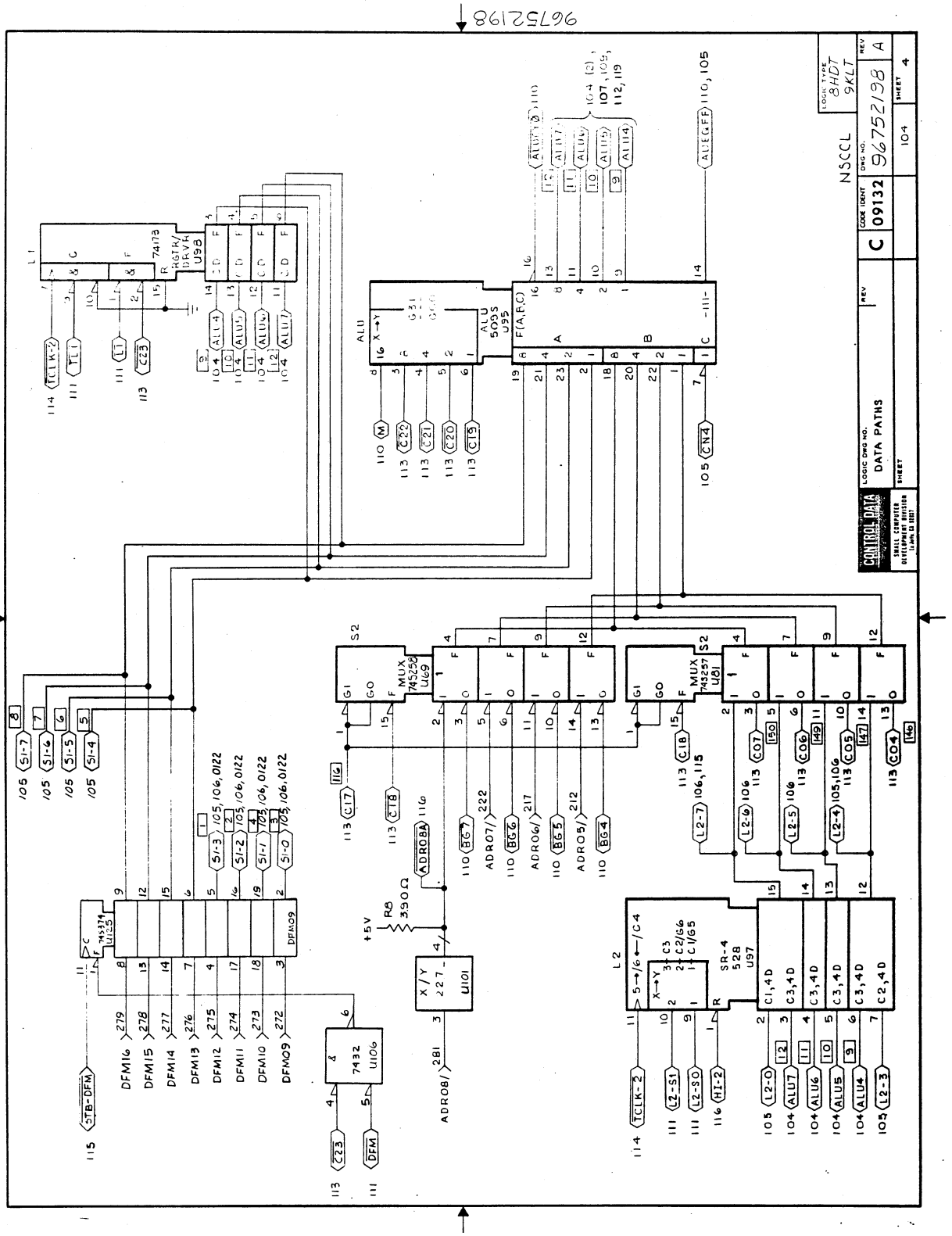


Figure 5-3. Primary BCLA Logic Diagram (Sheet 4 of 21)

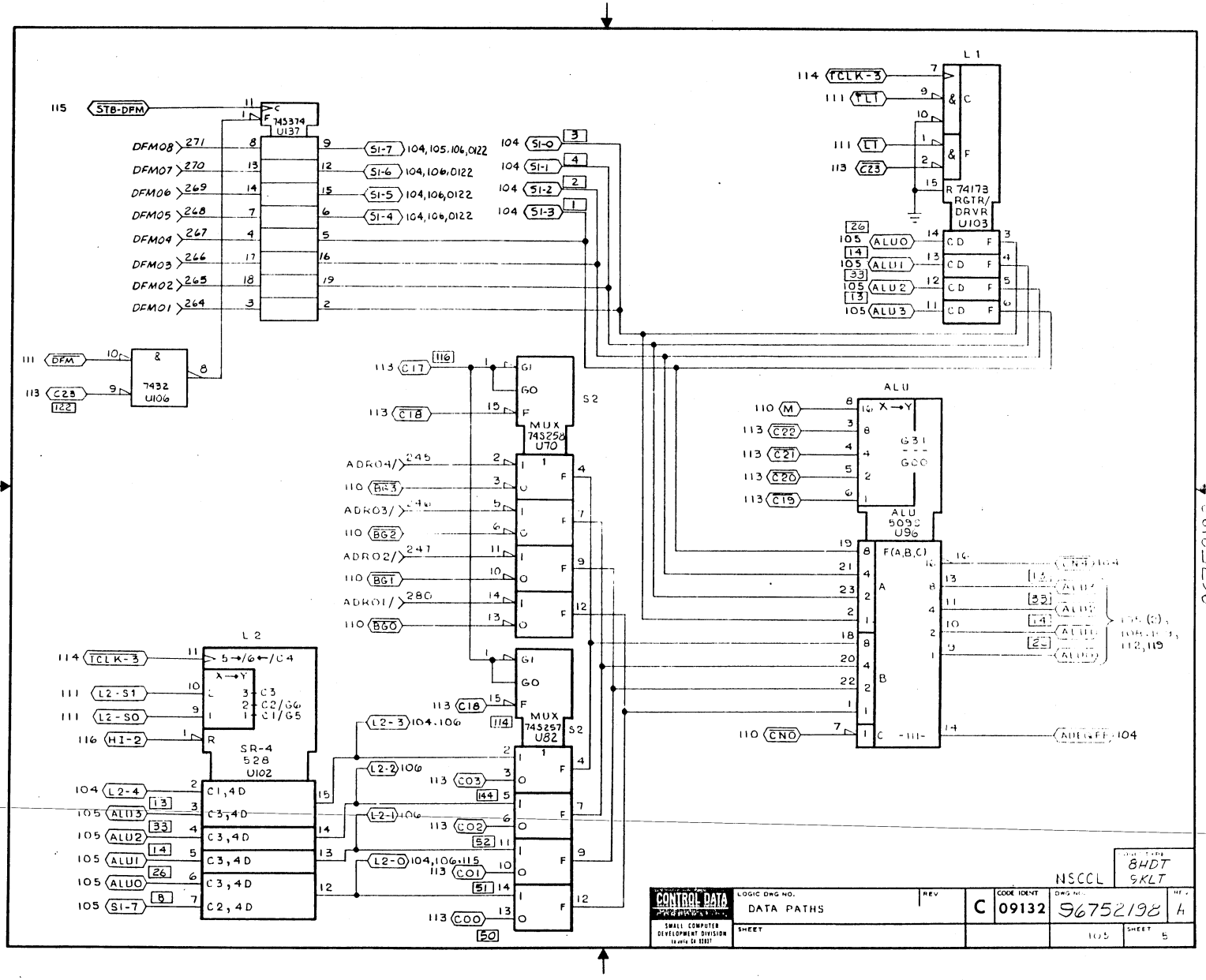
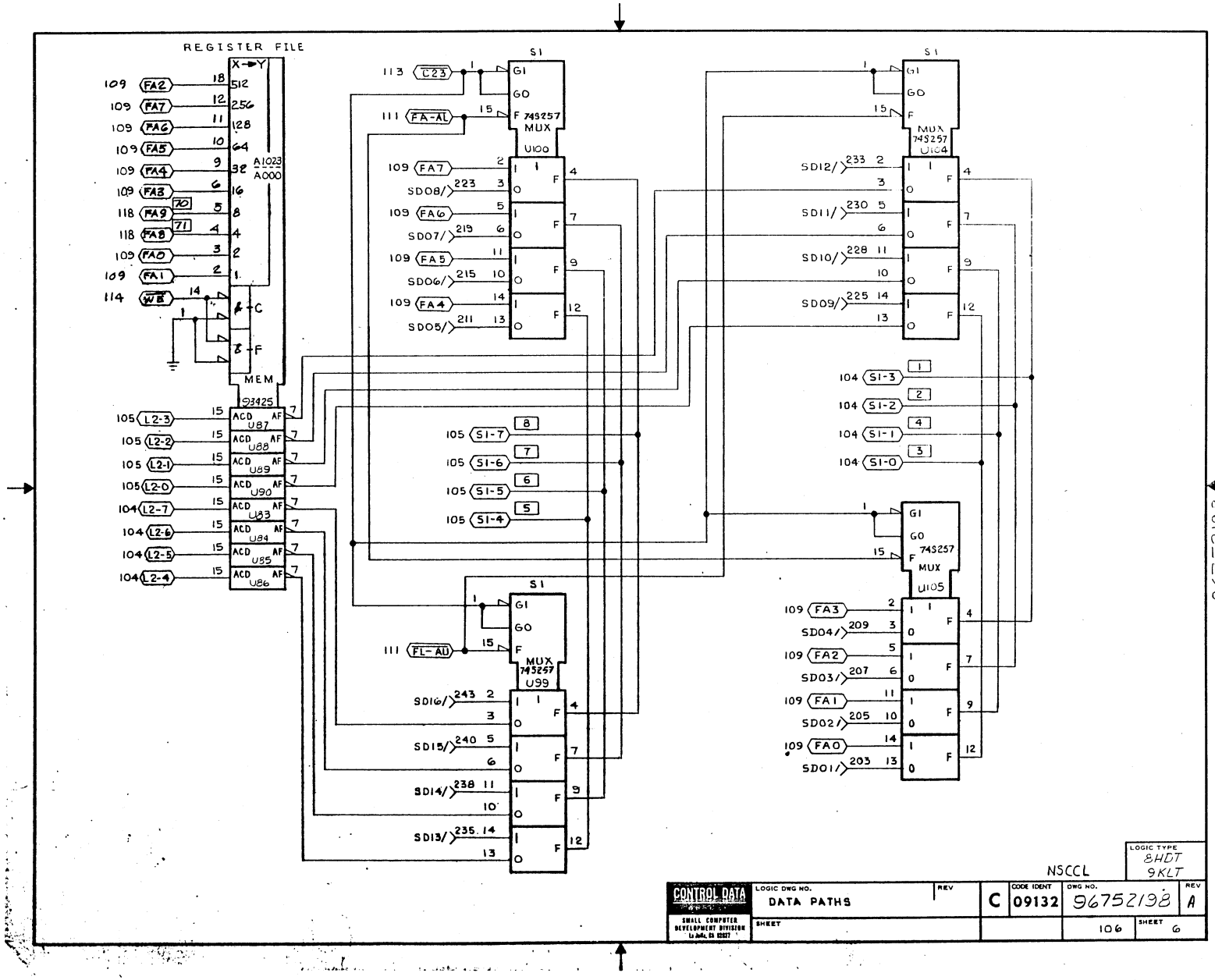


Figure 5-3. Primary BCLA Logic Diagram (Sheet 5 of 21)



96752198

Figure 5-3. Primary BCLA Logic Diagram (Sheet 6 of 21)

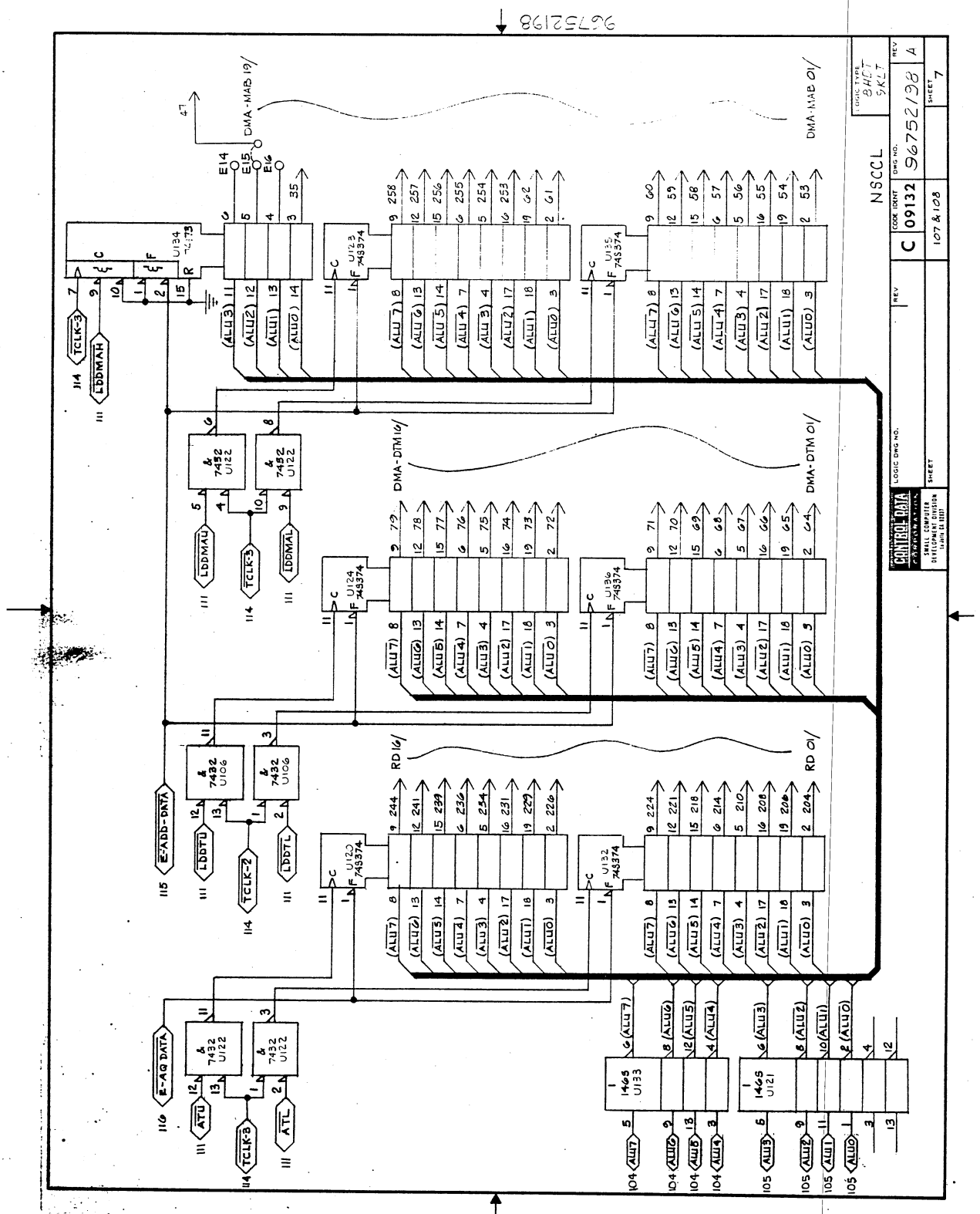


Figure 5-3. Primary BCLA Logic Diagram (Sheet 7 of 21)

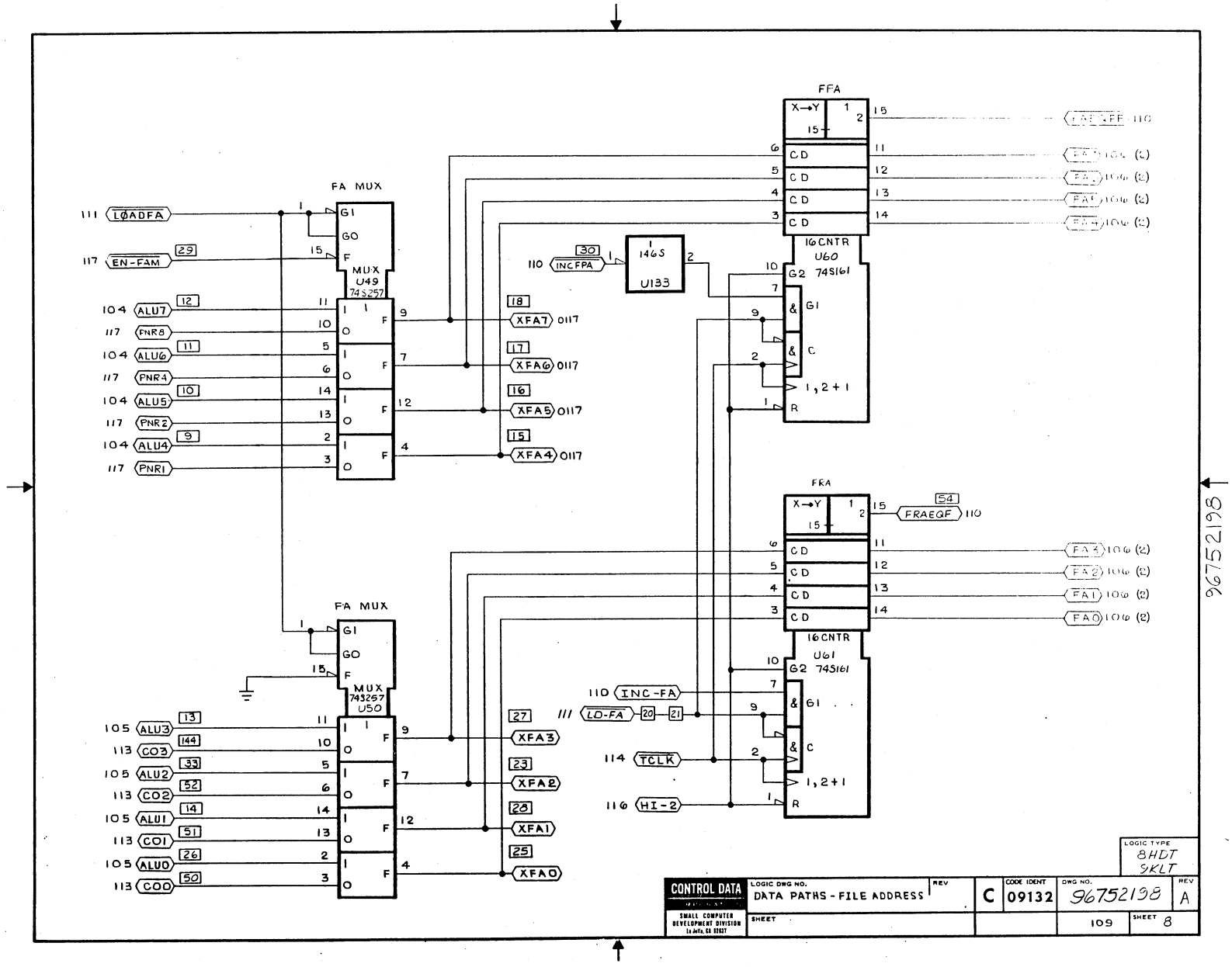
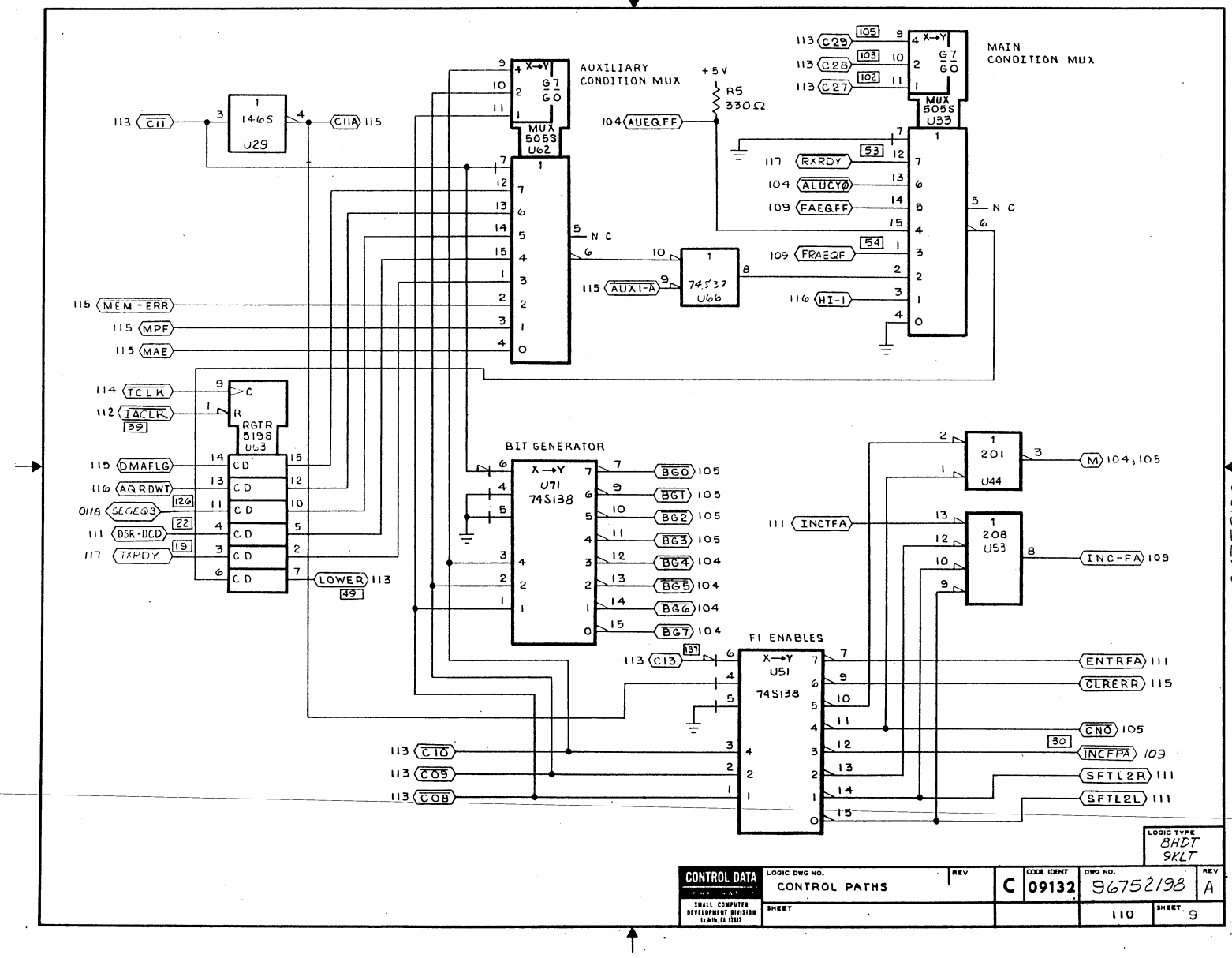


Figure 5-3. Primary BCLA Logic Diagram (Sheet 8 of 21)



96752198 A

Figure 5-3. Primary BCLA Logic Diagram (Sheet 9 of 21)

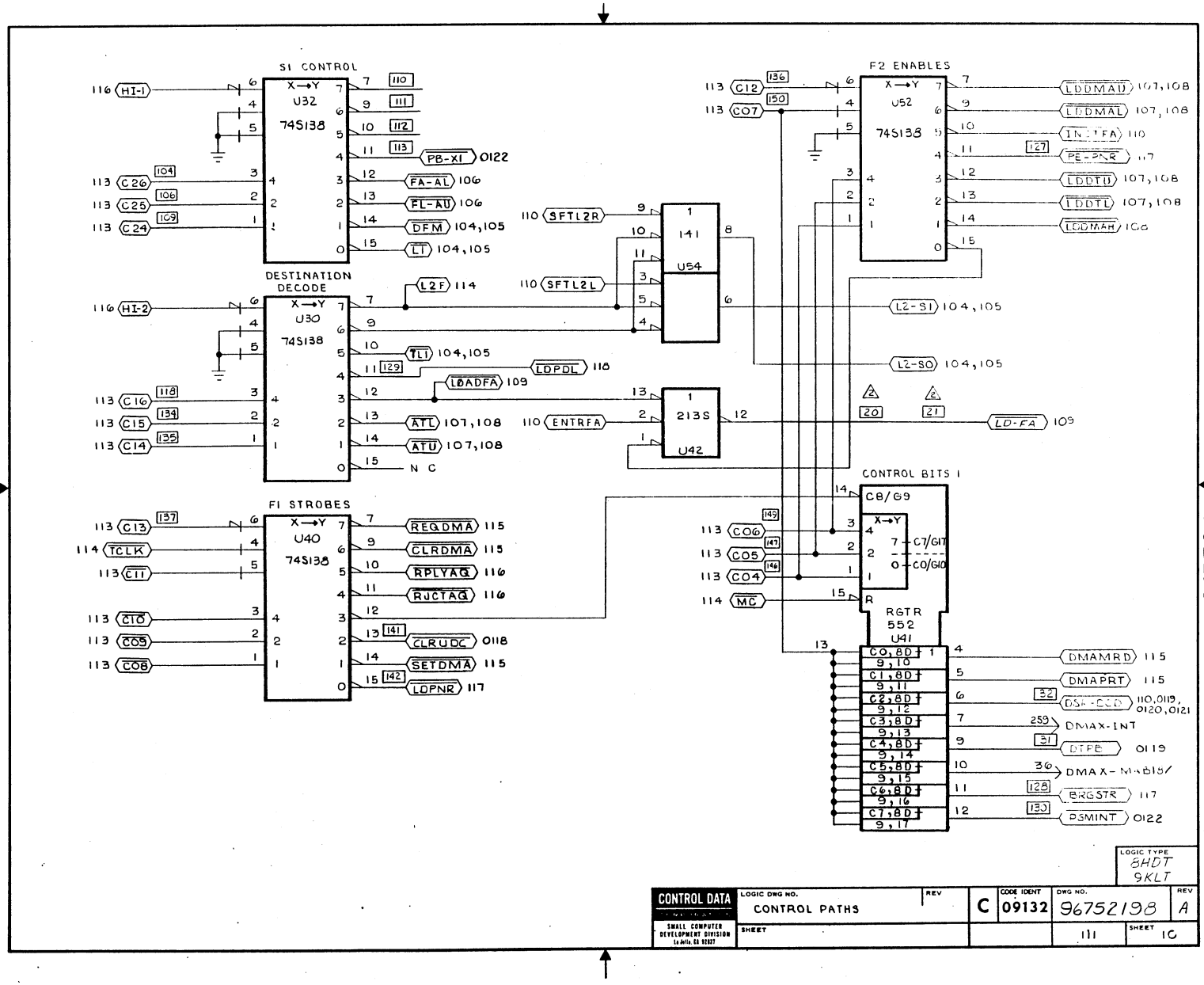
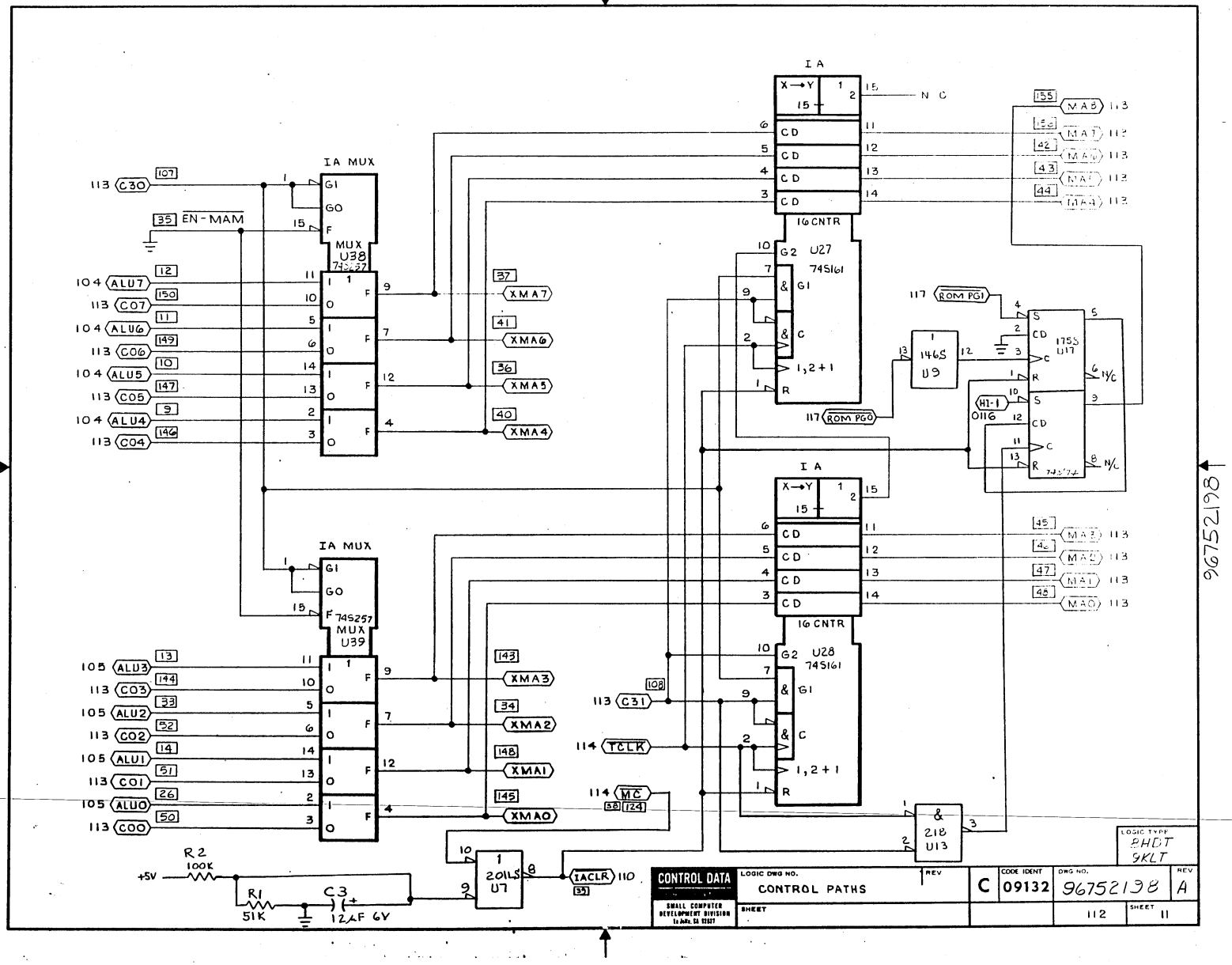


Figure 5-3. Primary BCLA Logic Diagram (Sheet 10 of 21)



96752198

Figure 5-3. Primary BCLA Logic Diagram (Sheet 11 of 21)

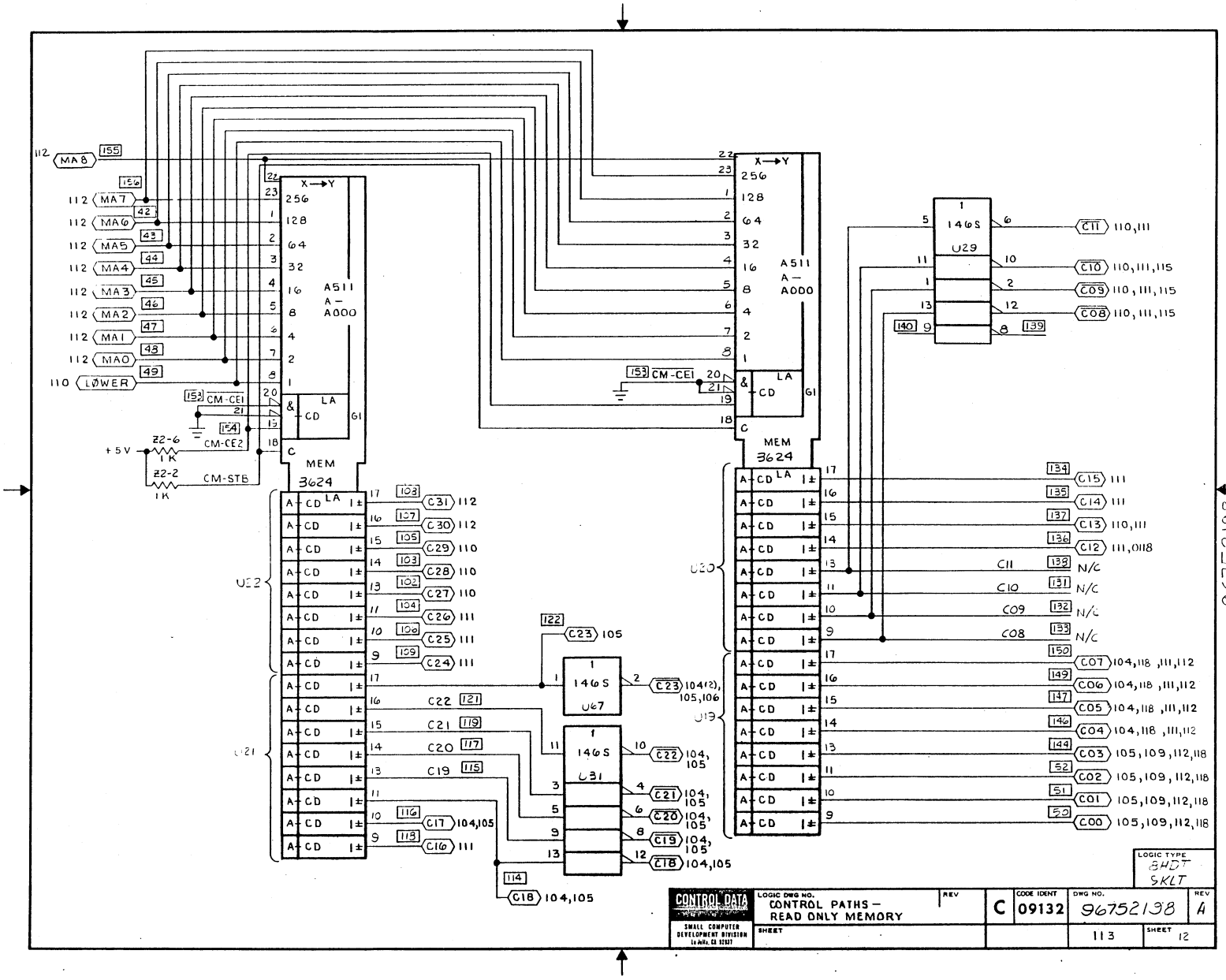


Figure 5-3. Primary BCLA Logic Diagram (Sheet 12 of 21)

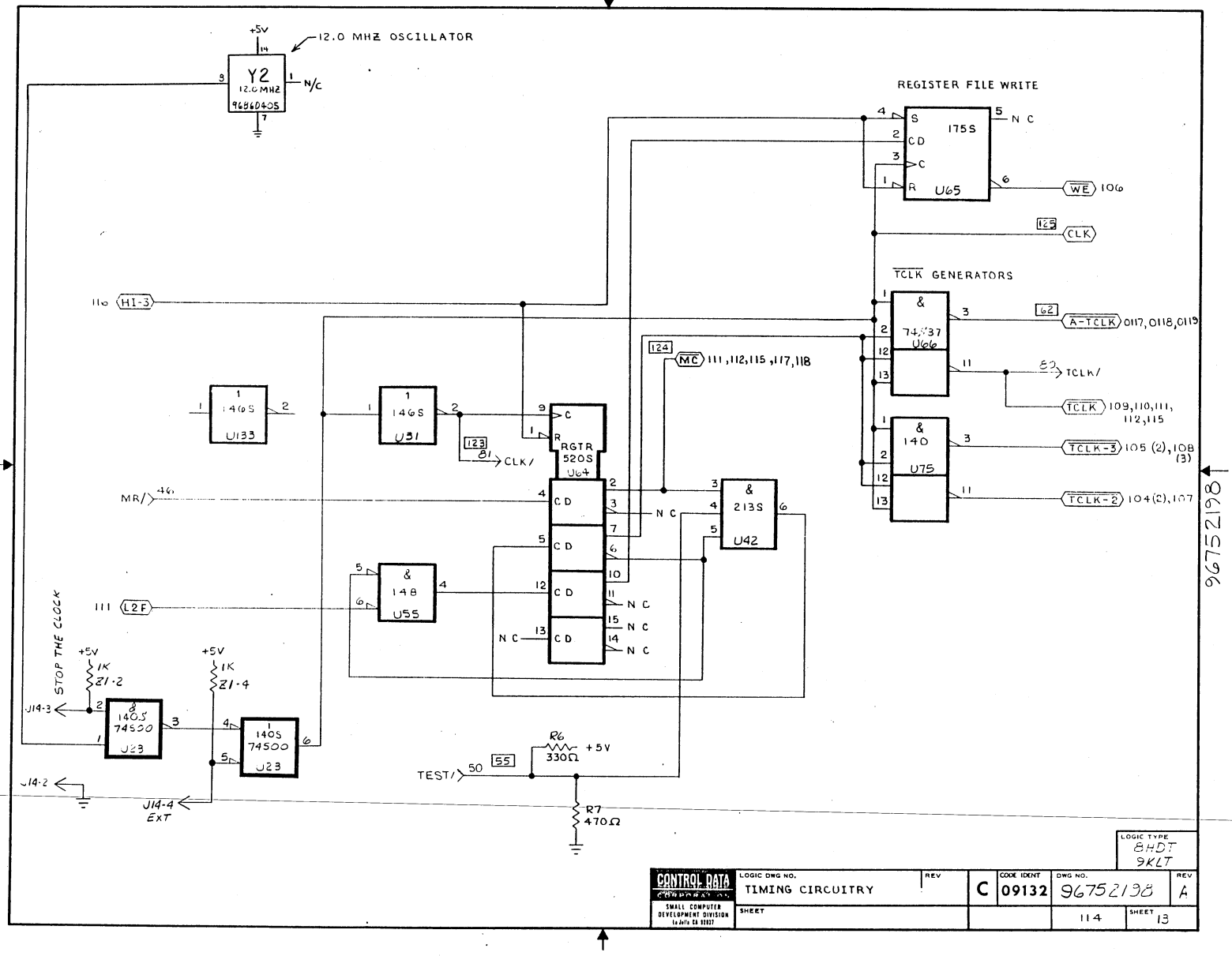
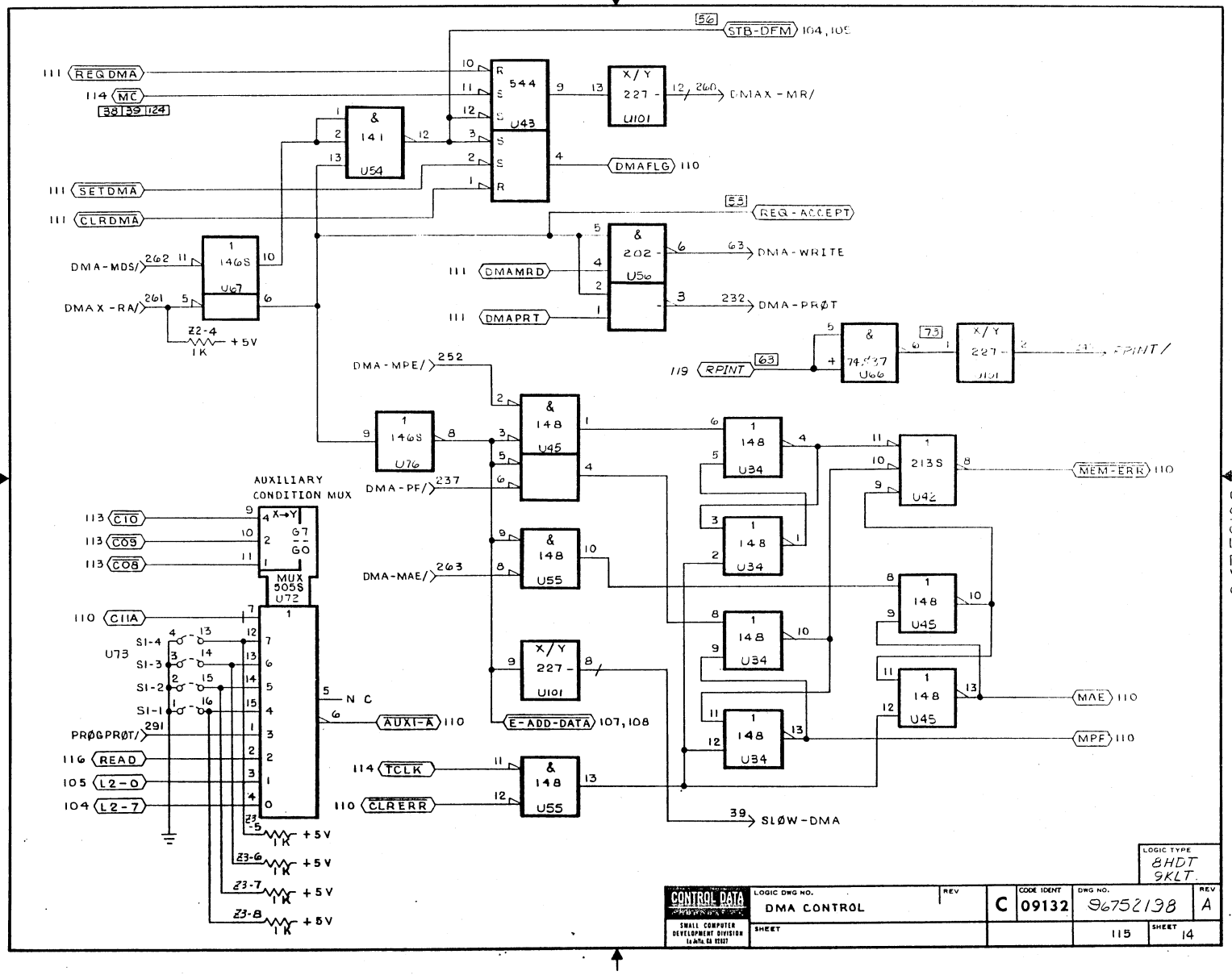


Figure 5-3. Primary BCLA Logic Diagram (Sheet 13 of 21)



96752198

Figure 5-3. Primary BCLA Logic Diagram (Sheet 14 of 21)

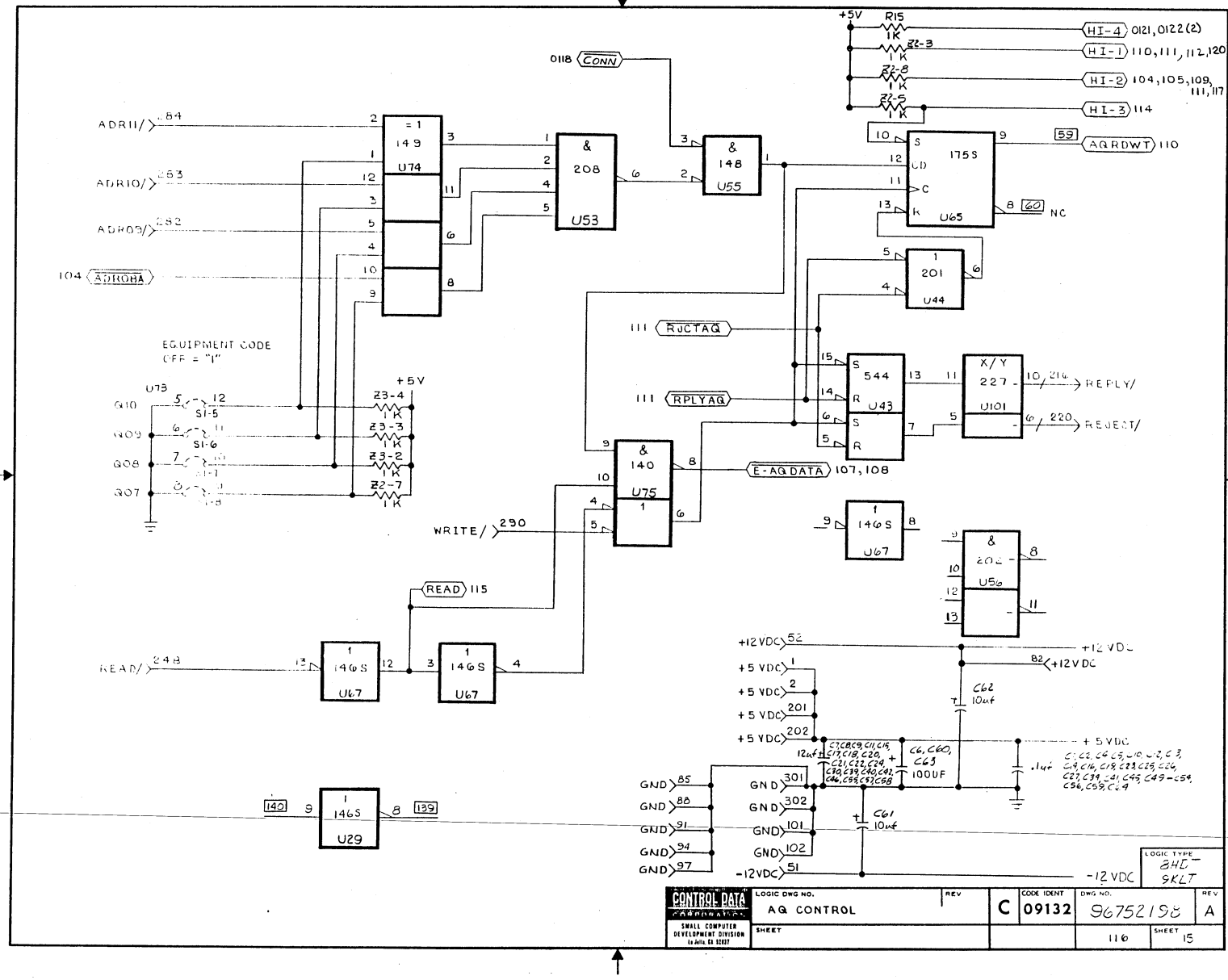


Figure 5-3. Primary BCLA Logic Diagram (Sheet 15 of 21)

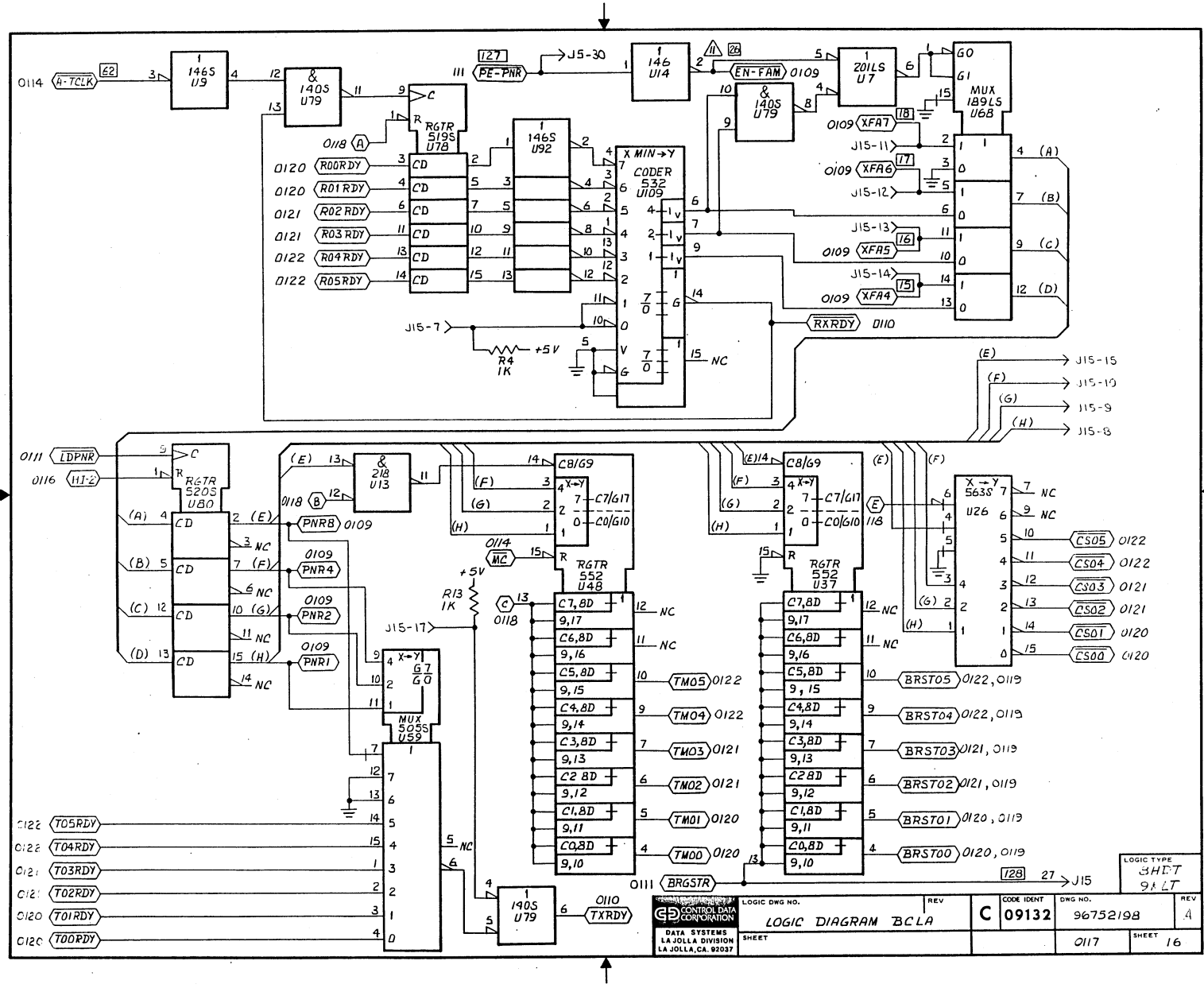
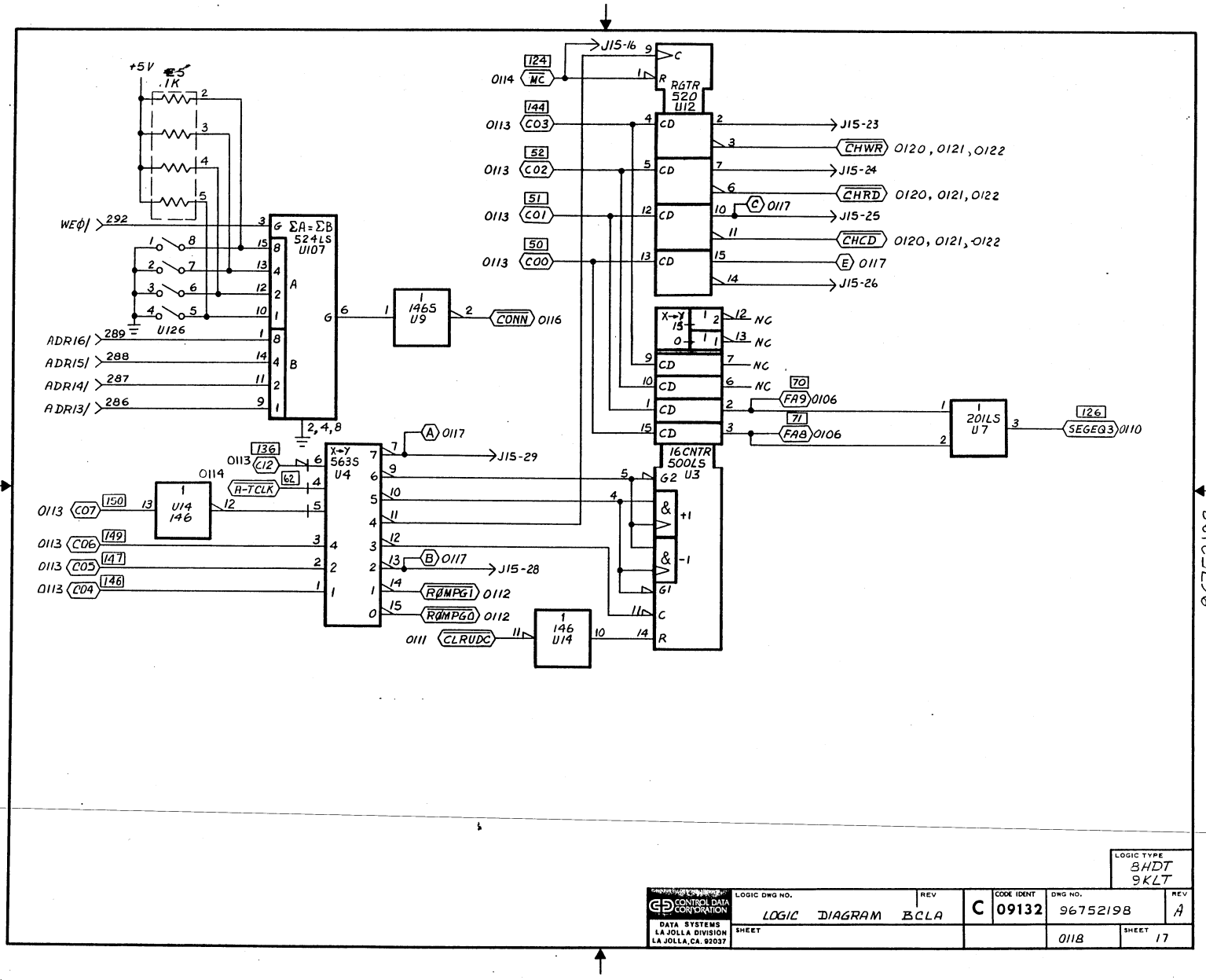


Figure 5-3. Primary BCLA Logic Diagram (Sheet 16 of 21)



96752198

Figure 5-3. Primary BCLA Logic Diagram (Sheet 17 of 21)

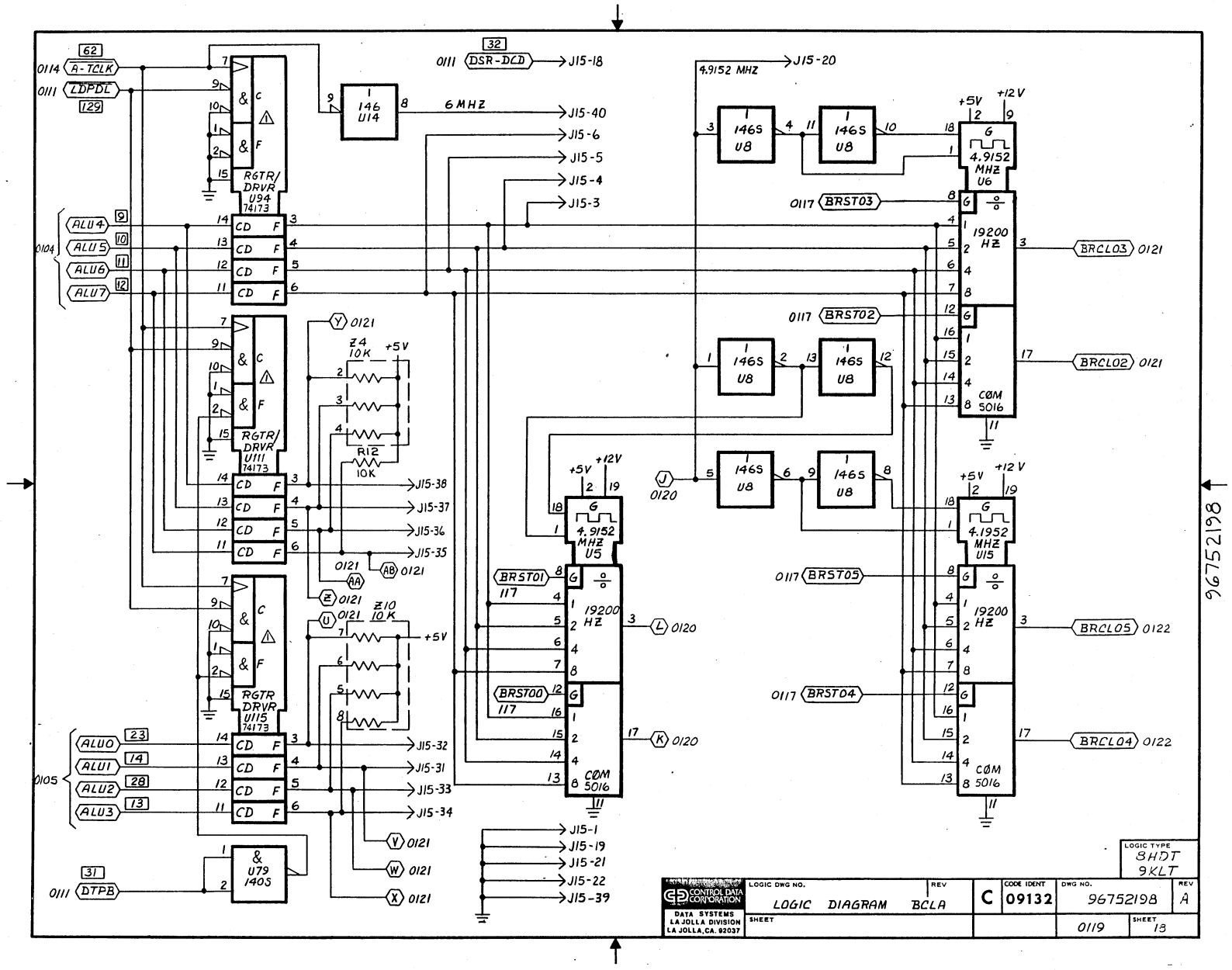


Figure 5-3. Primary BCLA Logic Diagram (Sheet 18 of 21)

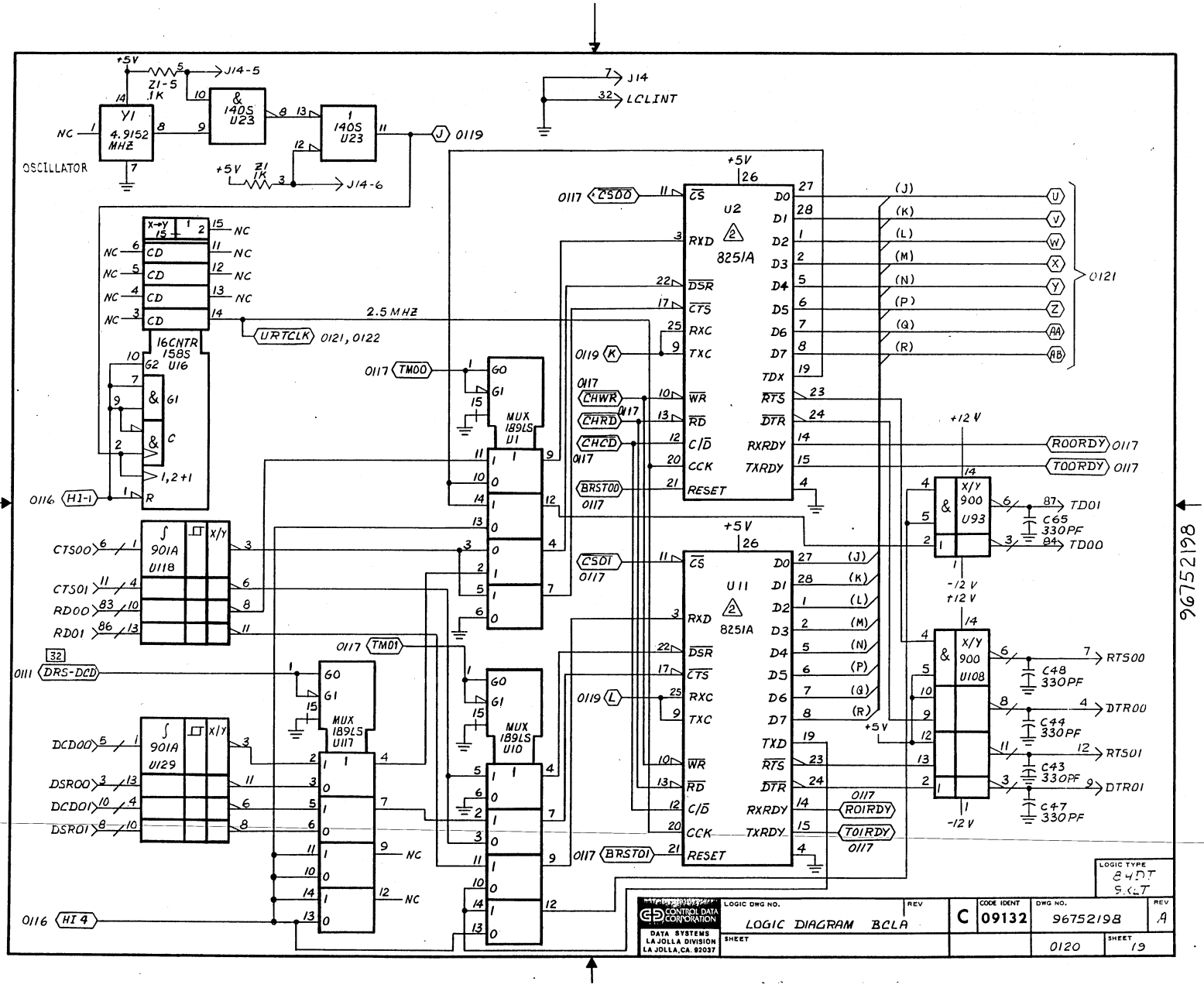


Figure 5-3. Primary BCLA Logic Diagram (Sheet 19 of 21)

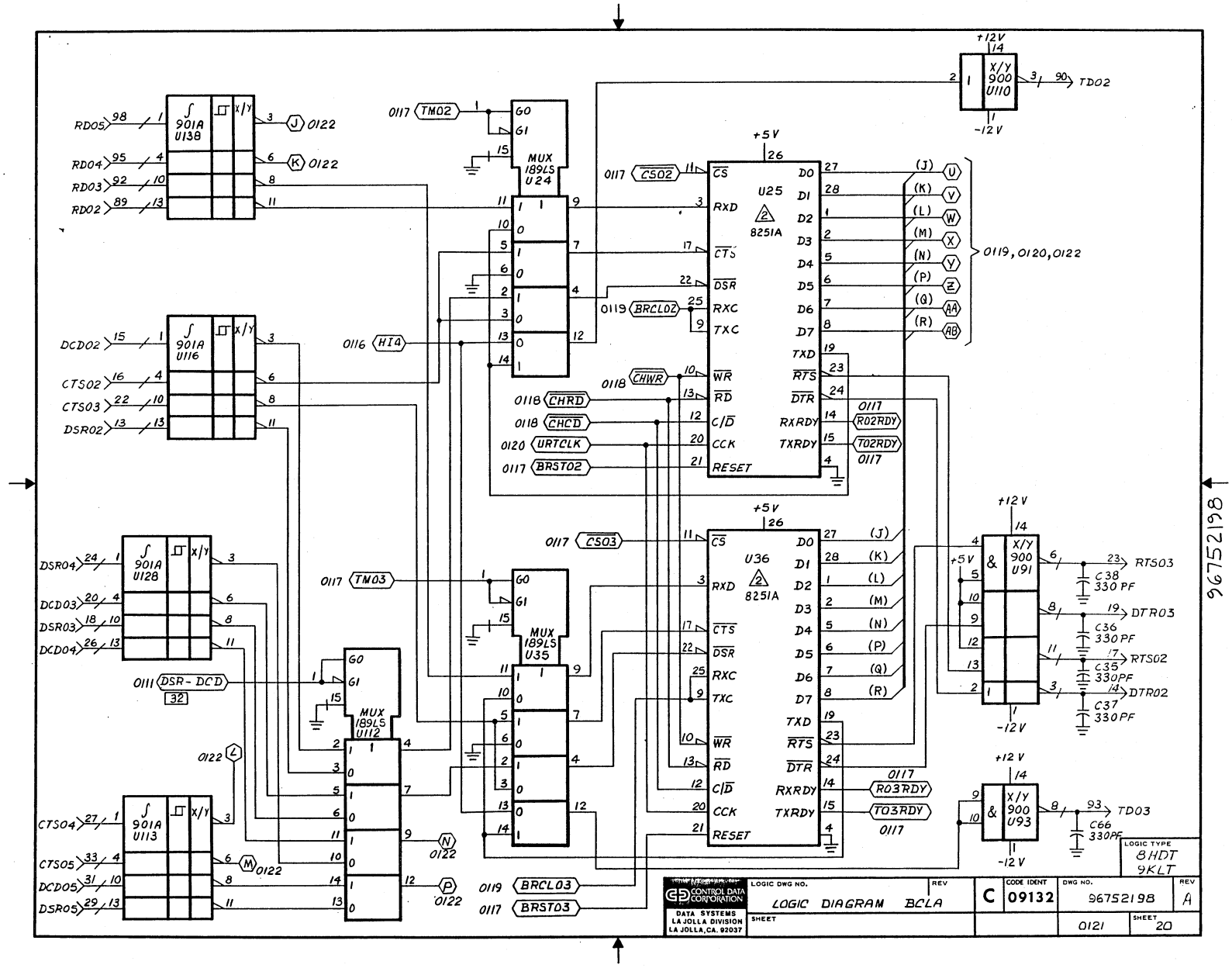


Figure 5-3. Primary BCLA Logic Diagram (Sheet 20 of 21)

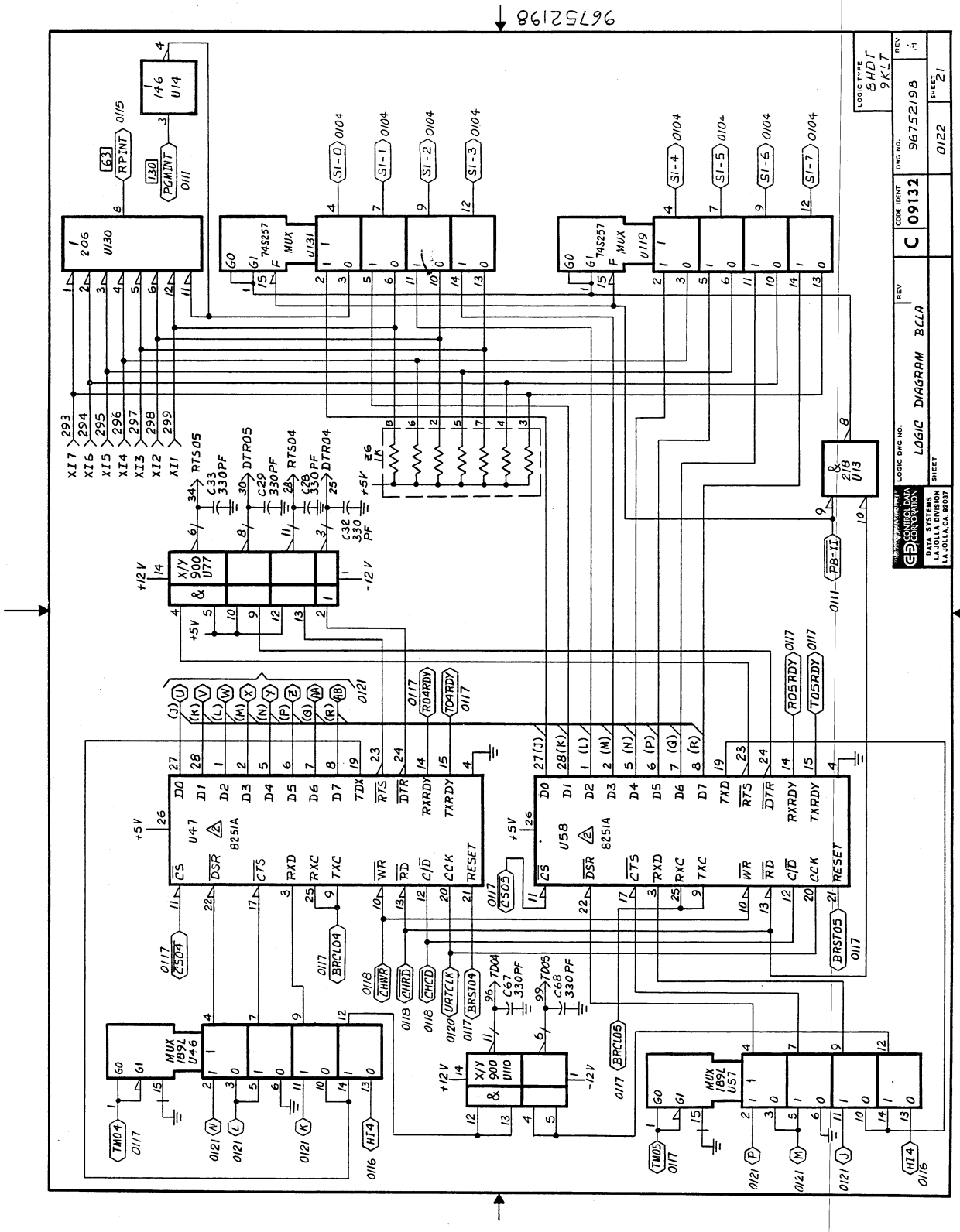


Figure 5-3. Primary BCLA Logic Diagram (Sheet 21 of 21)

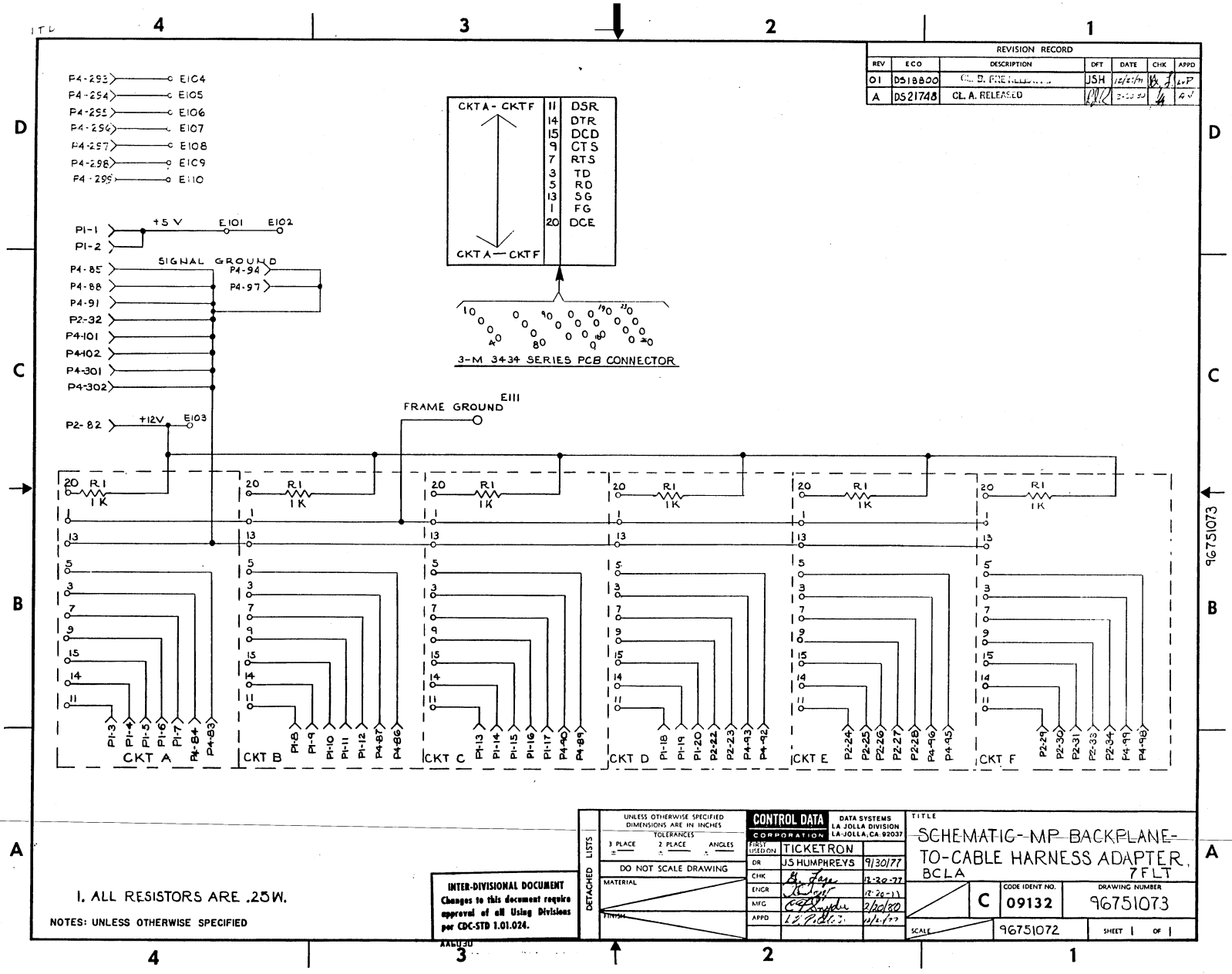
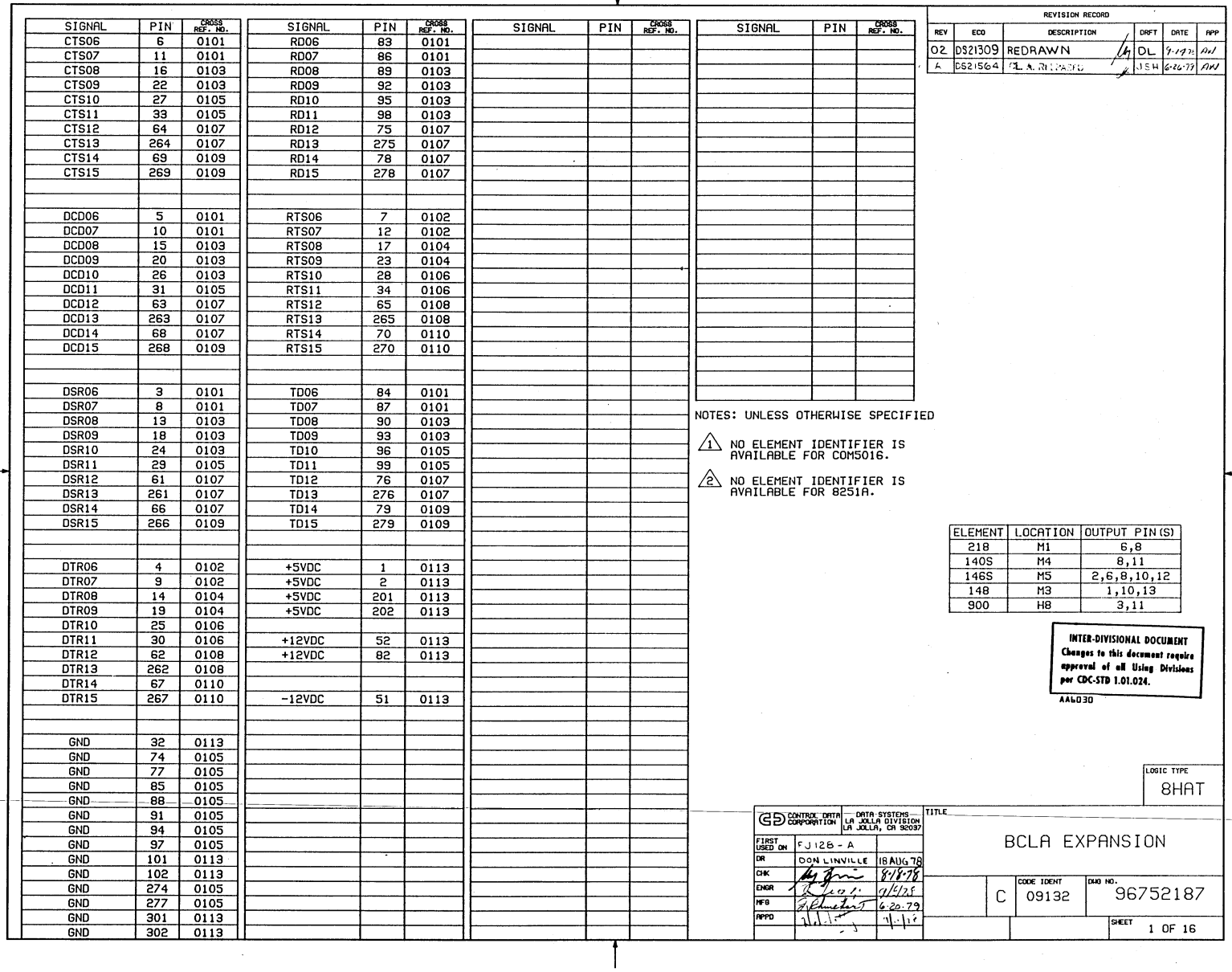


Figure 5-4. Primary BCLA Cable Harness Adapter Schematic Diagram



SIGNAL	PIN	CROSS REF. NO.
CTS06	6	0101
CTS07	11	0101
CTS08	16	0103
CTS09	22	0103
CTS10	27	0105
CTS11	33	0105
CTS12	64	0107
CTS13	264	0107
CTS14	69	0109
CTS15	269	0109
DCD06	5	0101
DCD07	10	0101
DCD08	15	0103
DCD09	20	0103
DCD10	26	0103
DCD11	31	0105
DCD12	63	0107
DCD13	263	0107
DCD14	68	0107
DCD15	268	0109
DSR06	3	0101
DSR07	8	0101
DSR08	13	0103
DSR09	18	0103
DSR10	24	0103
DSR11	29	0105
DSR12	61	0107
DSR13	261	0107
DSR14	66	0107
DSR15	266	0109
DTR06	4	0102
DTR07	9	0102
DTR08	14	0104
DTR09	19	0104
DTR10	25	0106
DTR11	30	0106
DTR12	62	0108
DTR13	262	0108
DTR14	67	0110
DTR15	267	0110
GND	32	0113
GND	74	0105
GND	77	0105
GND	85	0105
GND	88	0105
GND	91	0105
GND	94	0105
GND	97	0105
GND	101	0113
GND	102	0113
GND	274	0105
GND	277	0105
GND	301	0113
GND	302	0113

SIGNAL	PIN	CROSS REF. NO.
RD06	83	0101
RD07	86	0101
RD08	89	0103
RD09	92	0103
RD10	95	0103
RD11	98	0103
RD12	75	0107
RD13	275	0107
RD14	78	0107
RD15	278	0107
RTS06	7	0102
RTS07	12	0102
RTS08	17	0104
RTS09	23	0104
RTS10	28	0106
RTS11	34	0106
RTS12	65	0108
RTS13	265	0108
RTS14	70	0110
RTS15	270	0110
TD06	84	0101
TD07	87	0101
TD08	90	0103
TD09	93	0103
TD10	96	0105
TD11	99	0105
TD12	76	0107
TD13	276	0107
TD14	79	0109
TD15	279	0109
+5VDC	1	0113
+5VDC	2	0113
+5VDC	201	0113
+5VDC	202	0113
+12VDC	52	0113
+12VDC	82	0113
-12VDC	51	0113

SIGNAL	PIN	CROSS REF. NO.

SIGNAL	PIN	CROSS REF. NO.

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
02	DS21309	REDRAWN	DL	9-19-78	AM
A	DS21564	[illegible]	JSH	6-26-79	AM

NOTES: UNLESS OTHERWISE SPECIFIED

1. NO ELEMENT IDENTIFIER IS AVAILABLE FOR COM5016.
2. NO ELEMENT IDENTIFIER IS AVAILABLE FOR 8251A.

ELEMENT	LOCATION	OUTPUT PIN(S)
218	M1	6,8
140S	M4	8,11
146S	M5	2,6,8,10,12
148	M3	1,10,13
900	H8	3,11

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
AA6030

LOGIC TYPE 8HAT

CONTROL DATA CORPORATION — DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037

FIRST USED ON	FJ126-A	
DR	DON LINVILLE	18 AUG 78
CHK	[signature]	8/18/78
ENGR	[signature]	9/6/78
MFG	[signature]	6-20-79
APPD	[signature]	9-1-78

TITLE: BCLA EXPANSION

CODE IDENT	DWG NO.
09132	96752187

SIZE C — SHEET 1 OF 16

Figure 5-5. Expansion BCLA Logic Diagram (Sheet 1 of 16)

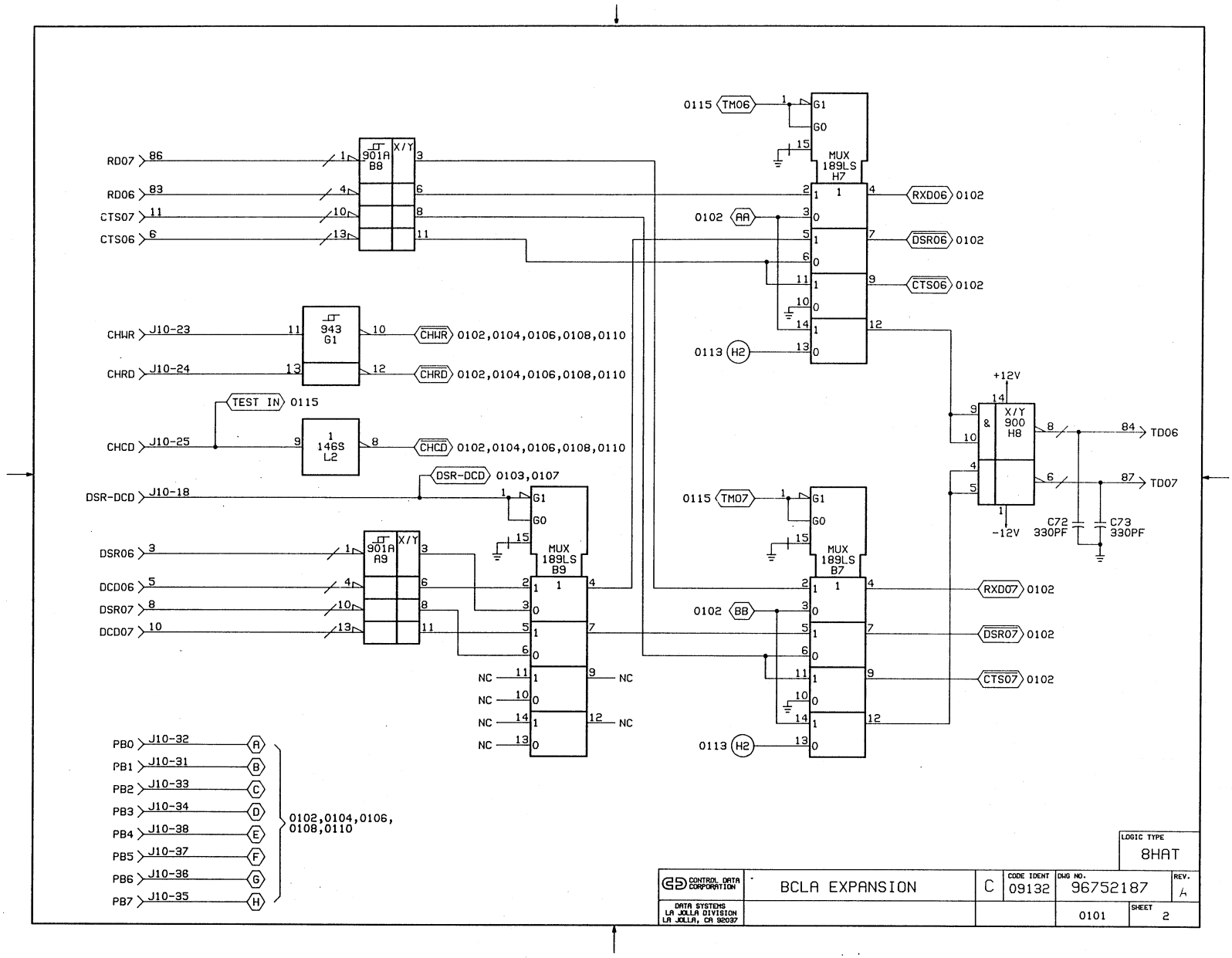


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 2 of 16)

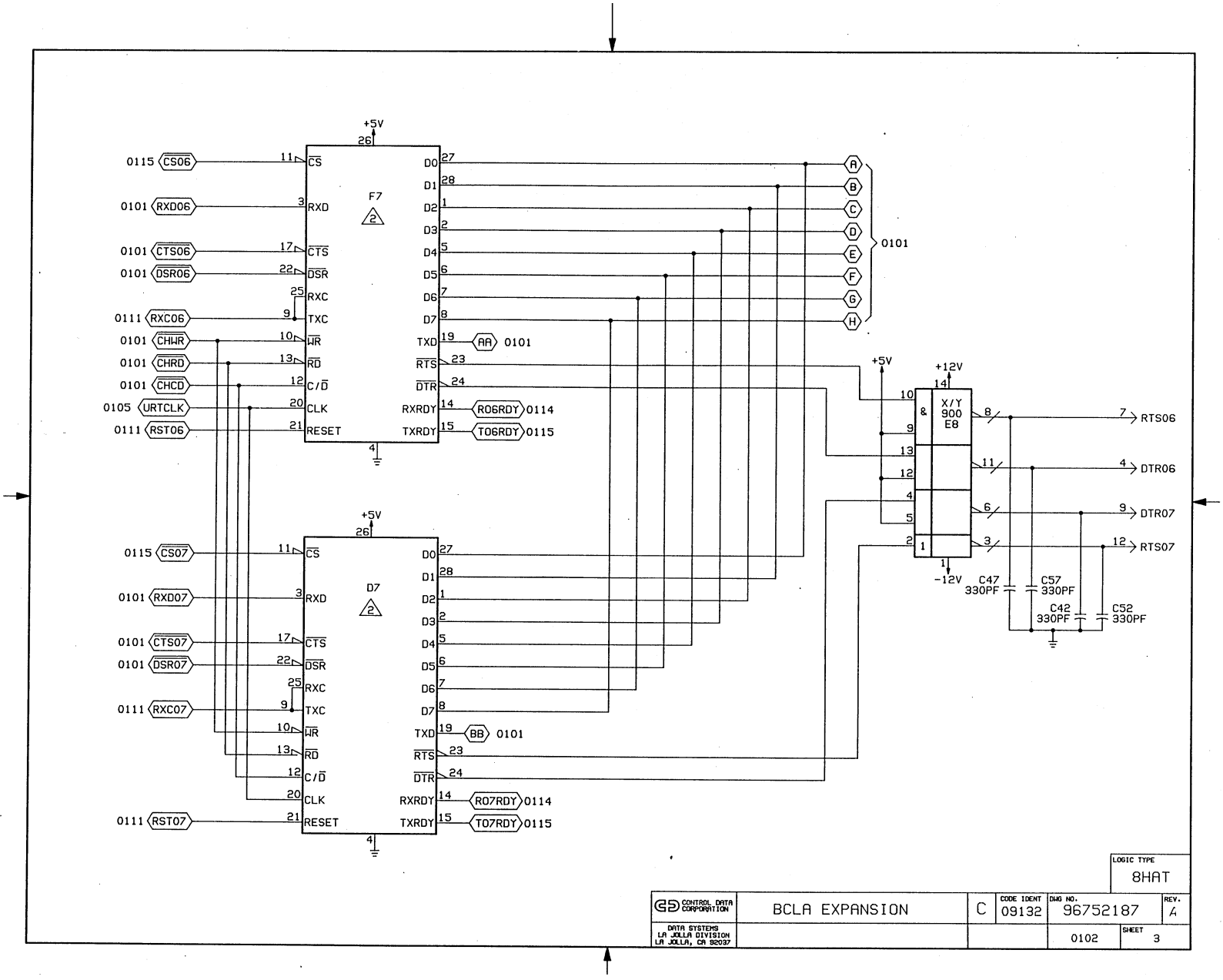


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 3 of 16)

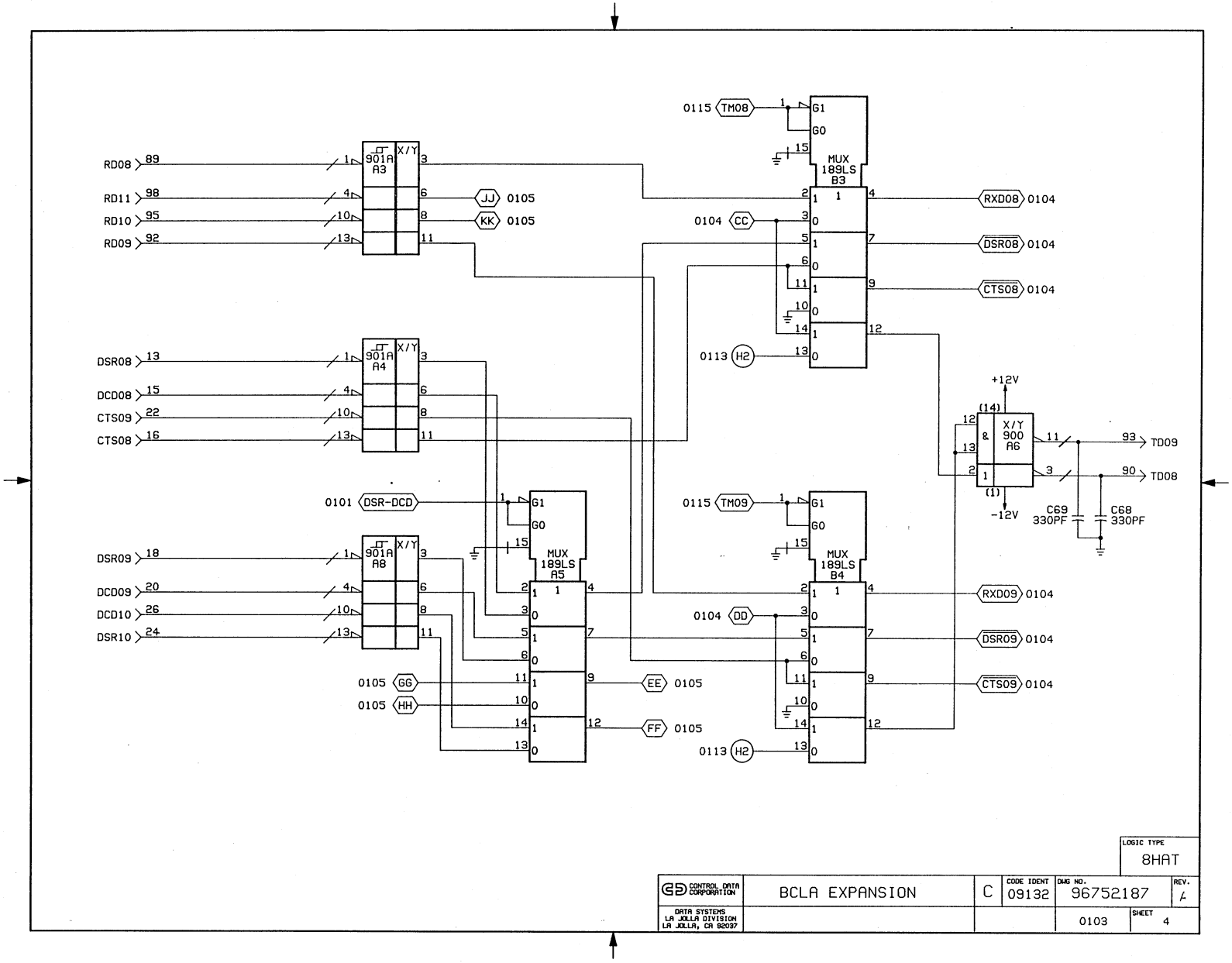


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 4 of 16)

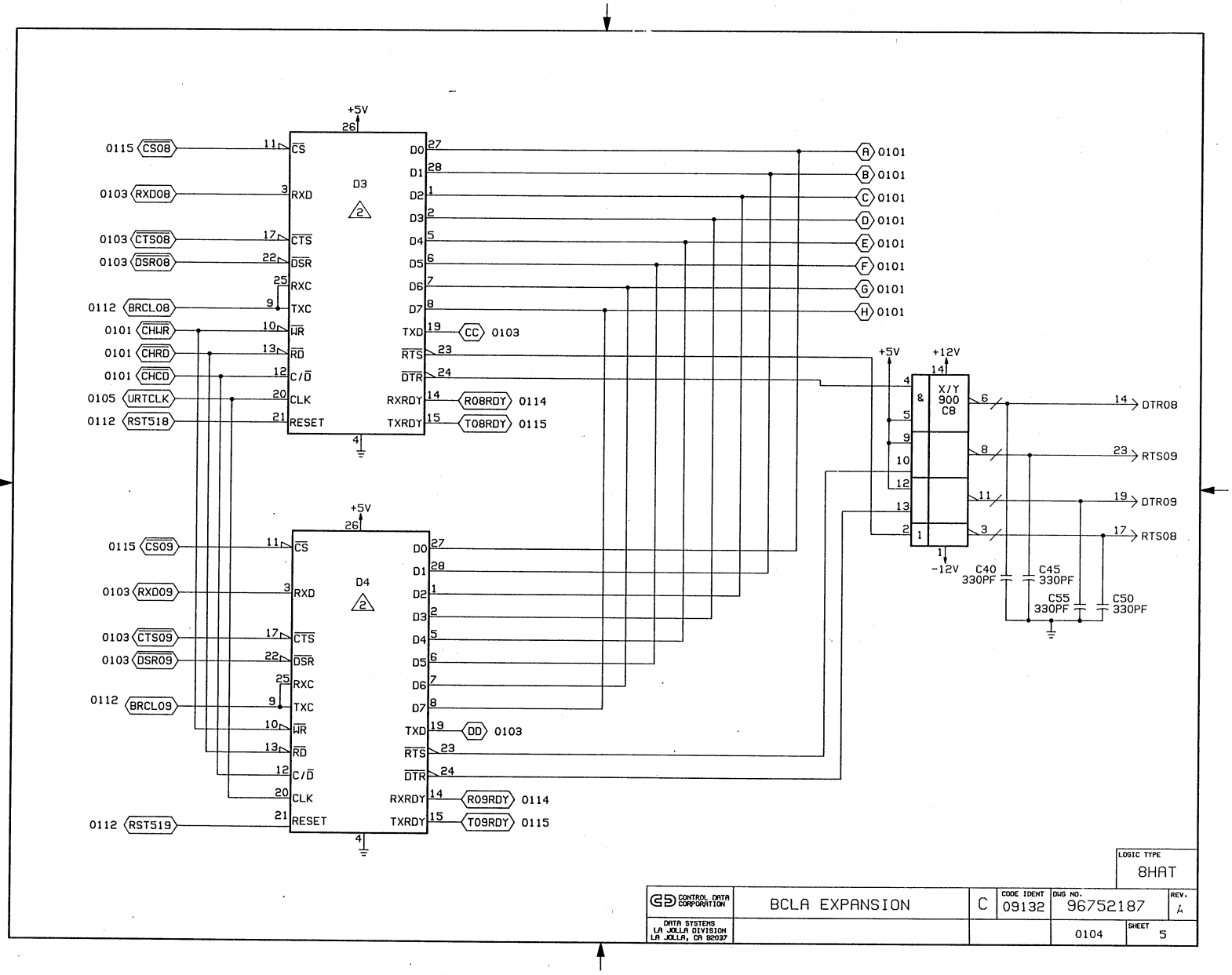


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 5 of 16)

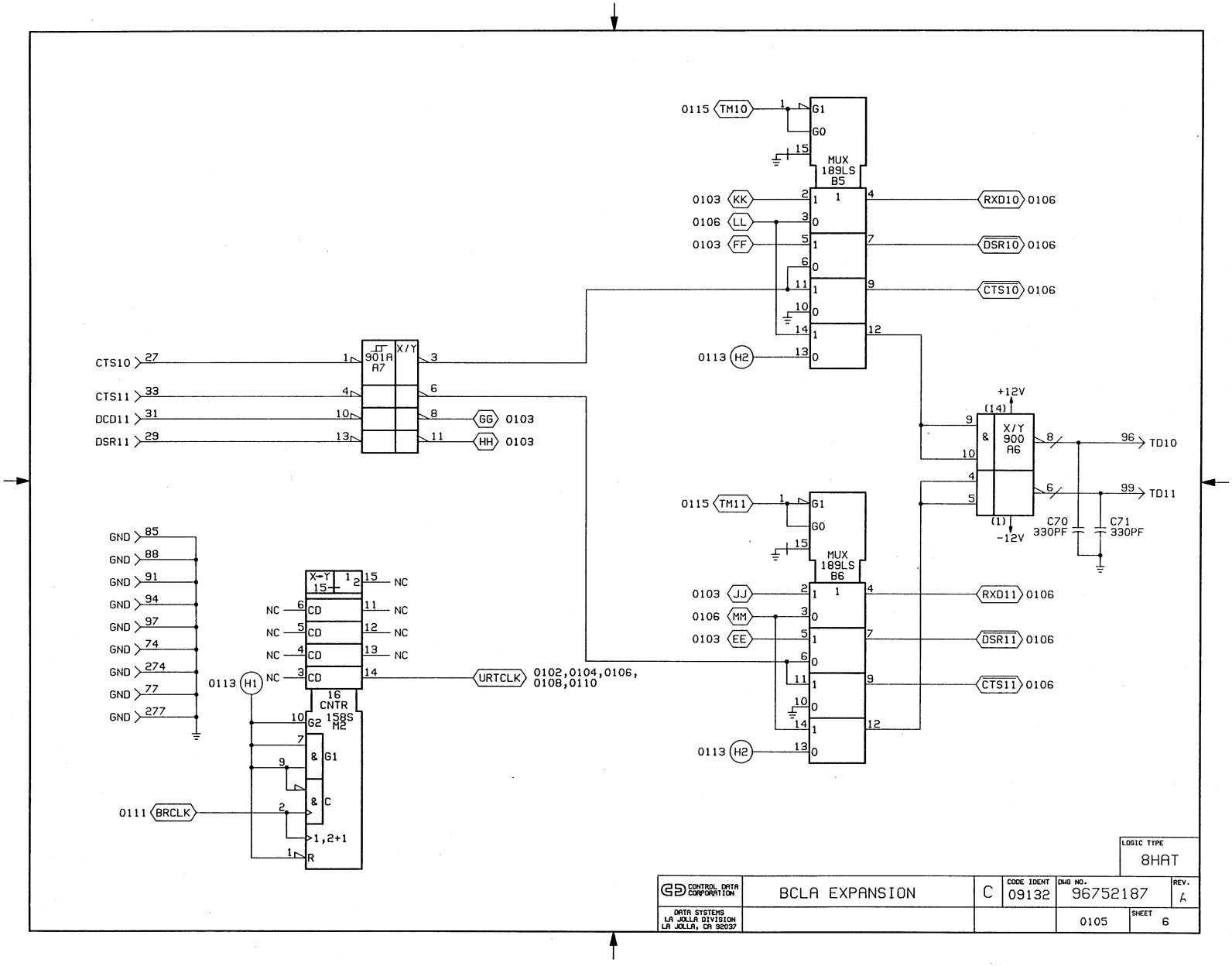


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 6 of 16)

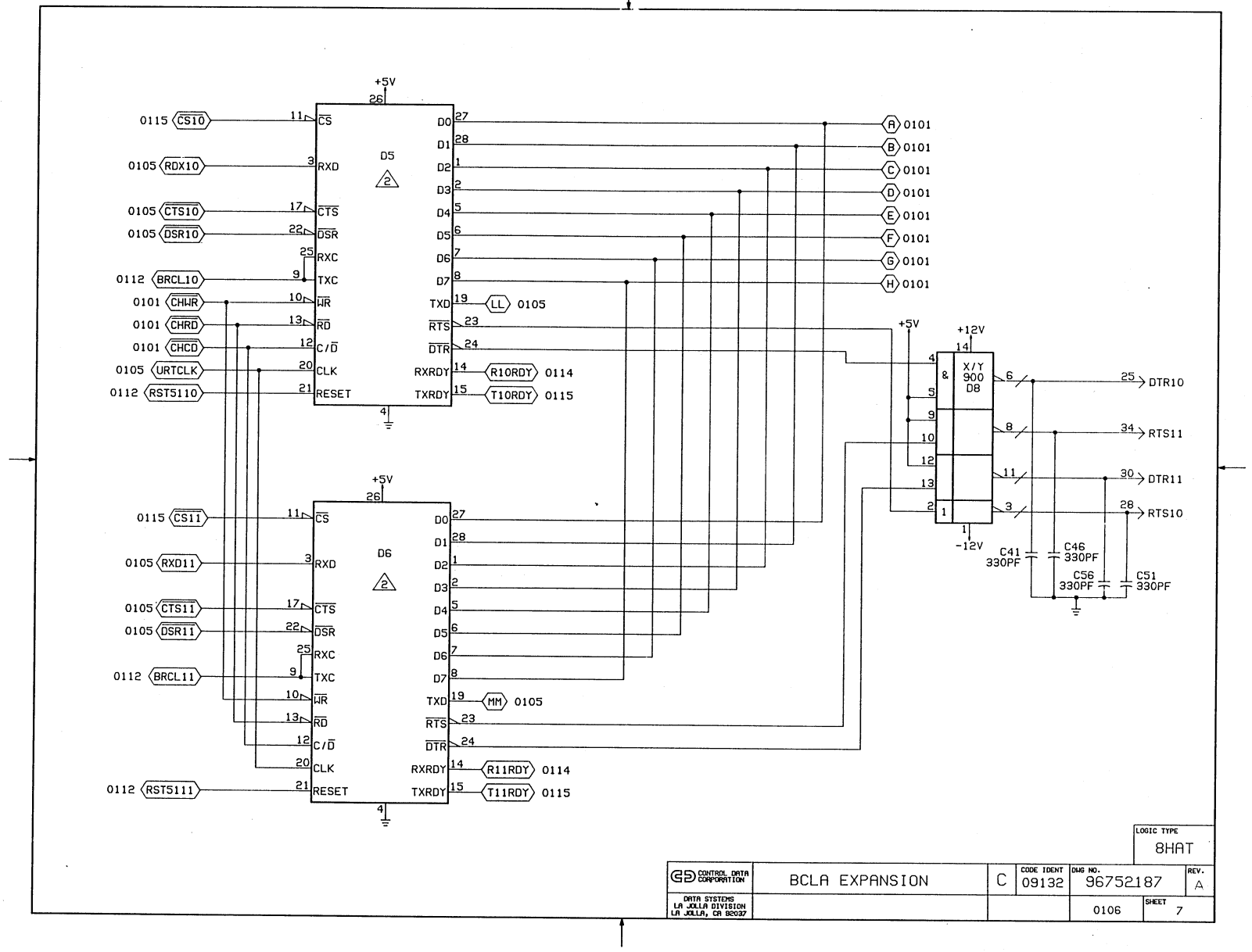


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 7 of 16)

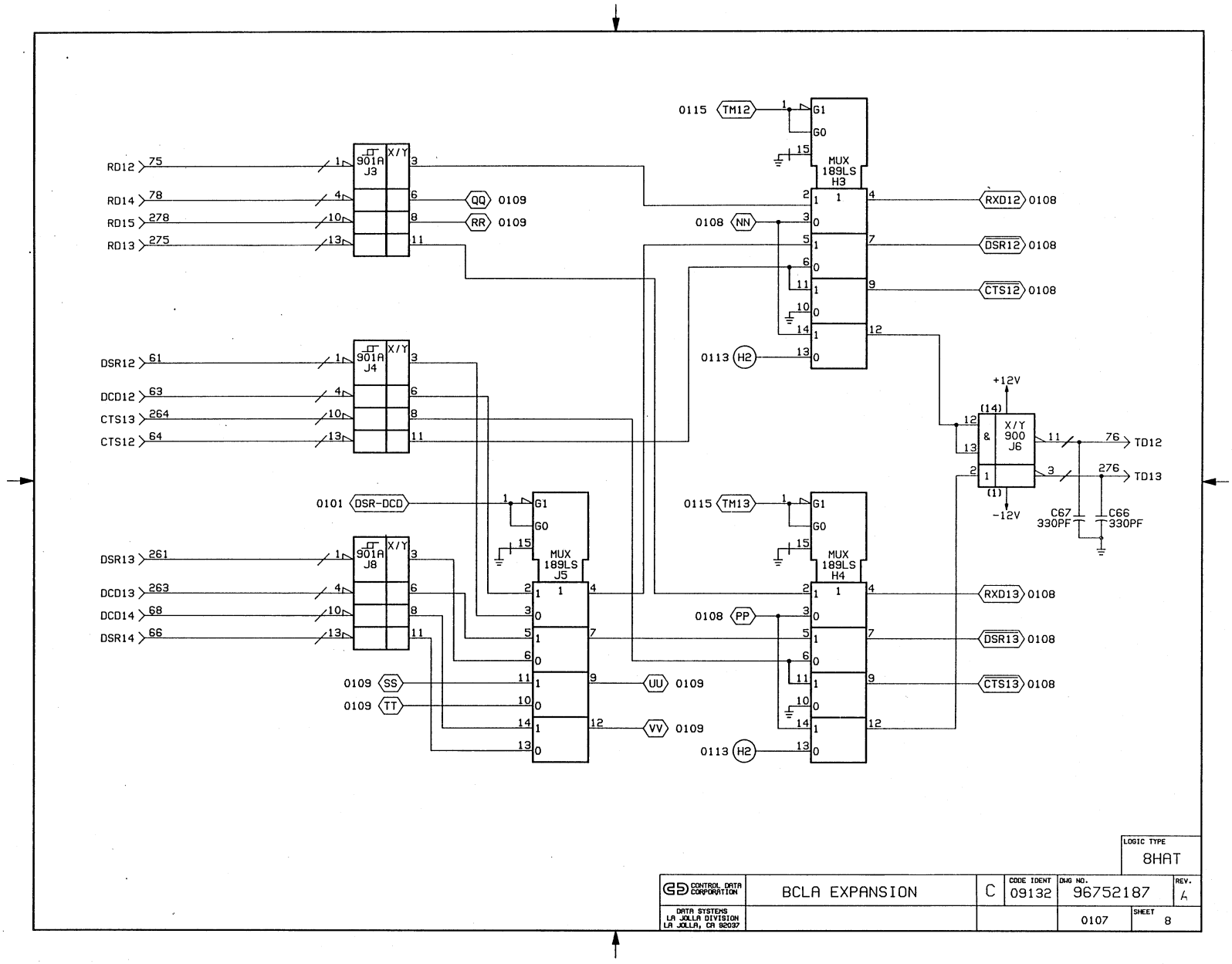


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 8 of 16)

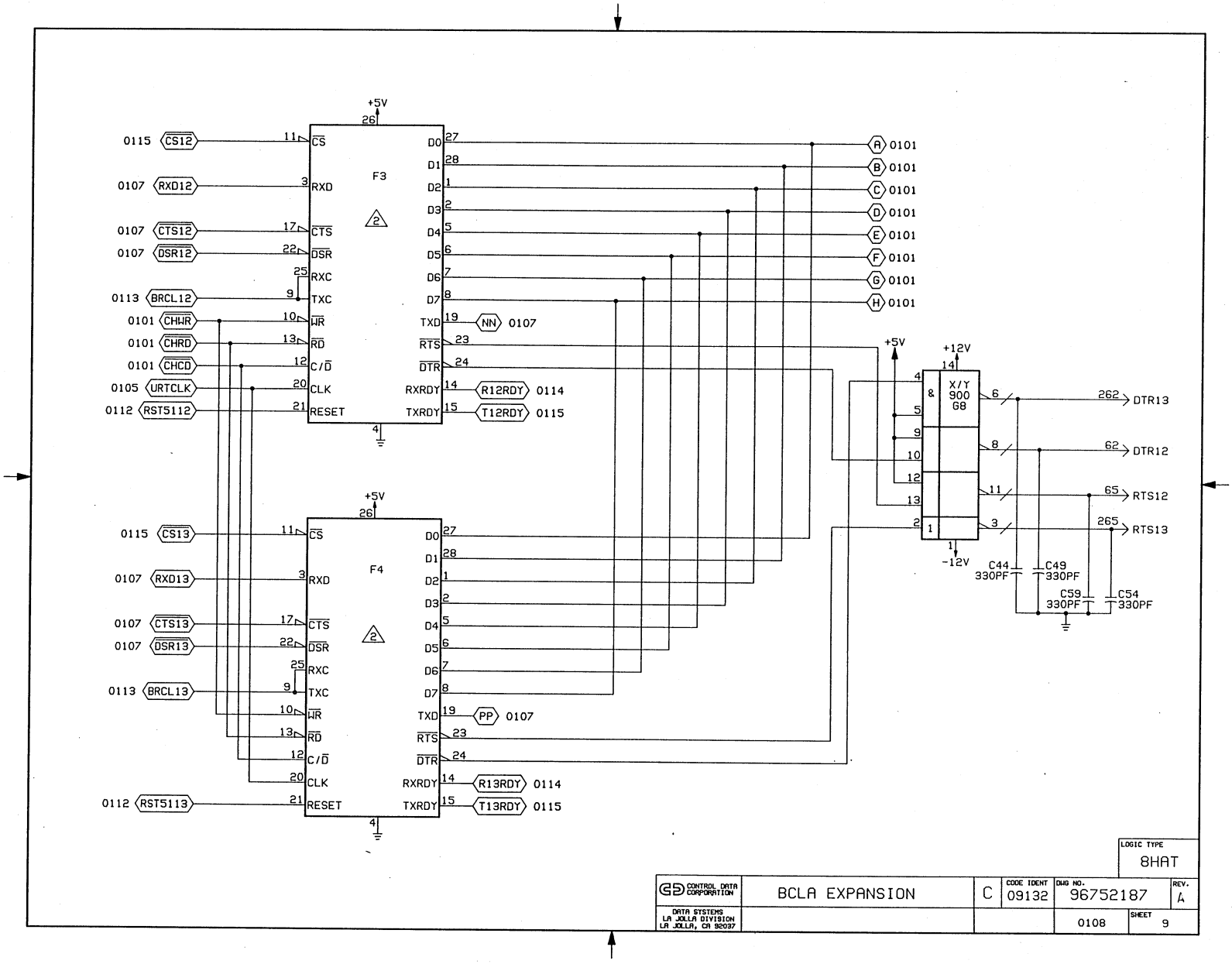


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 9 of 16)

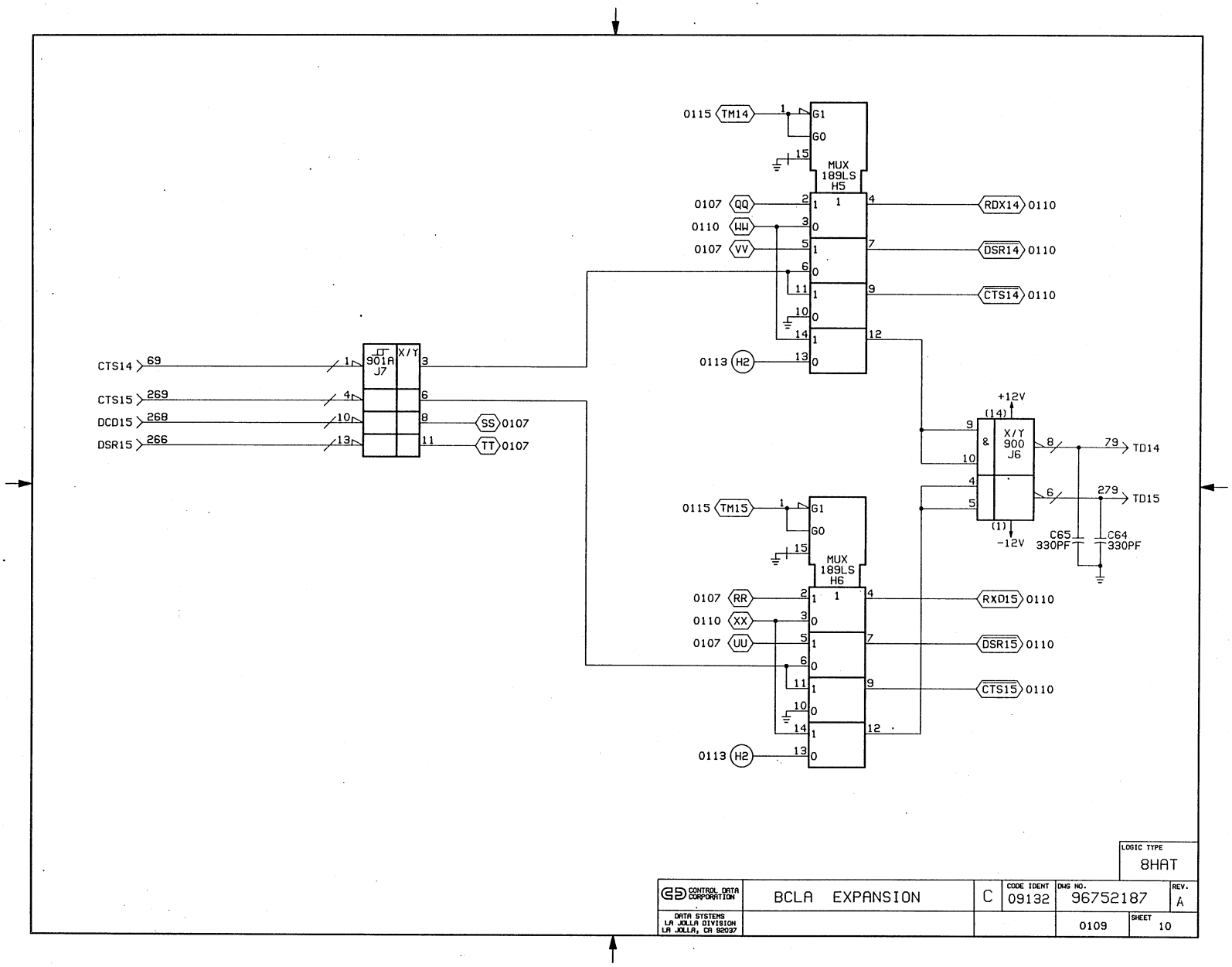


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 10 of 16)

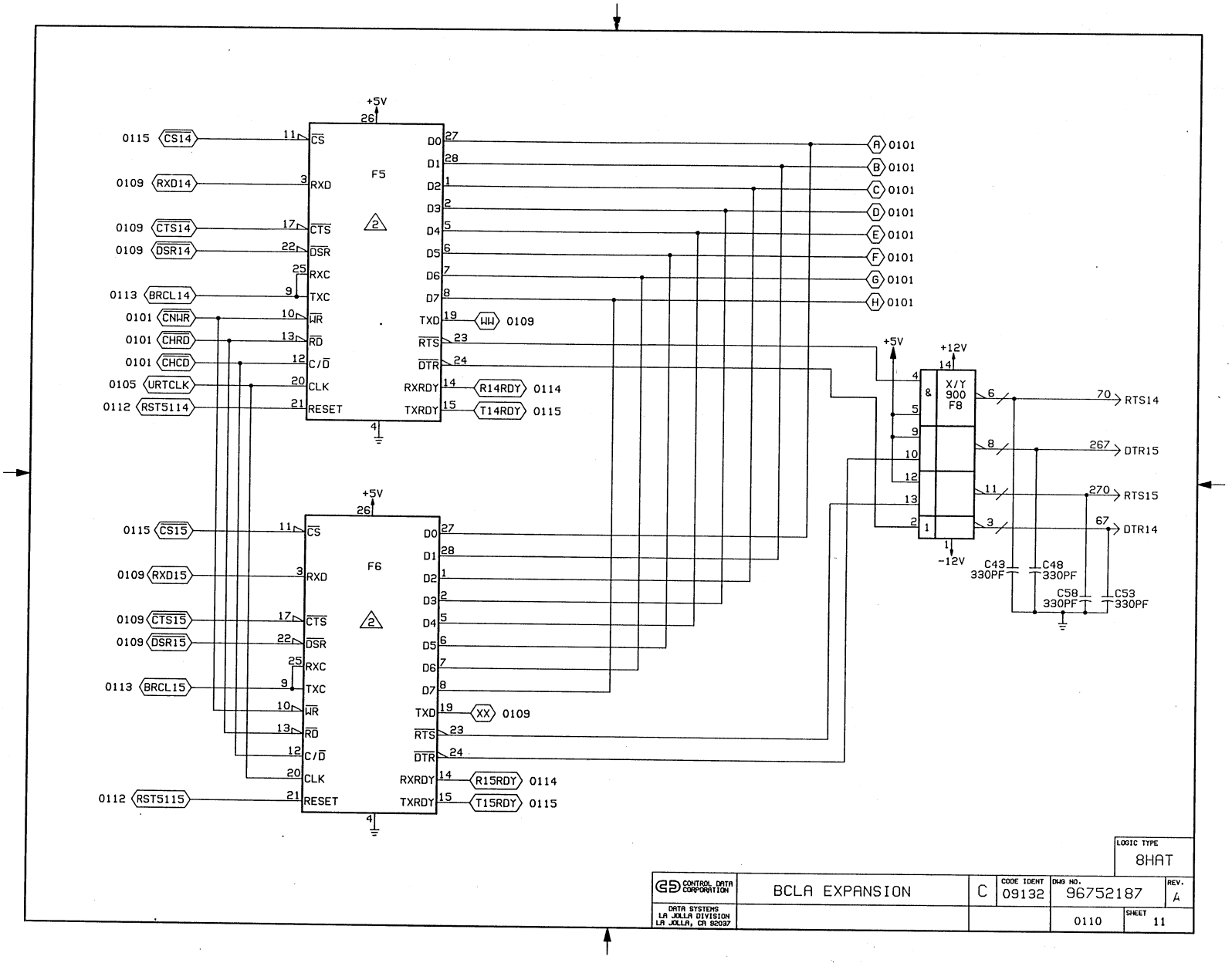


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 11 of 16)

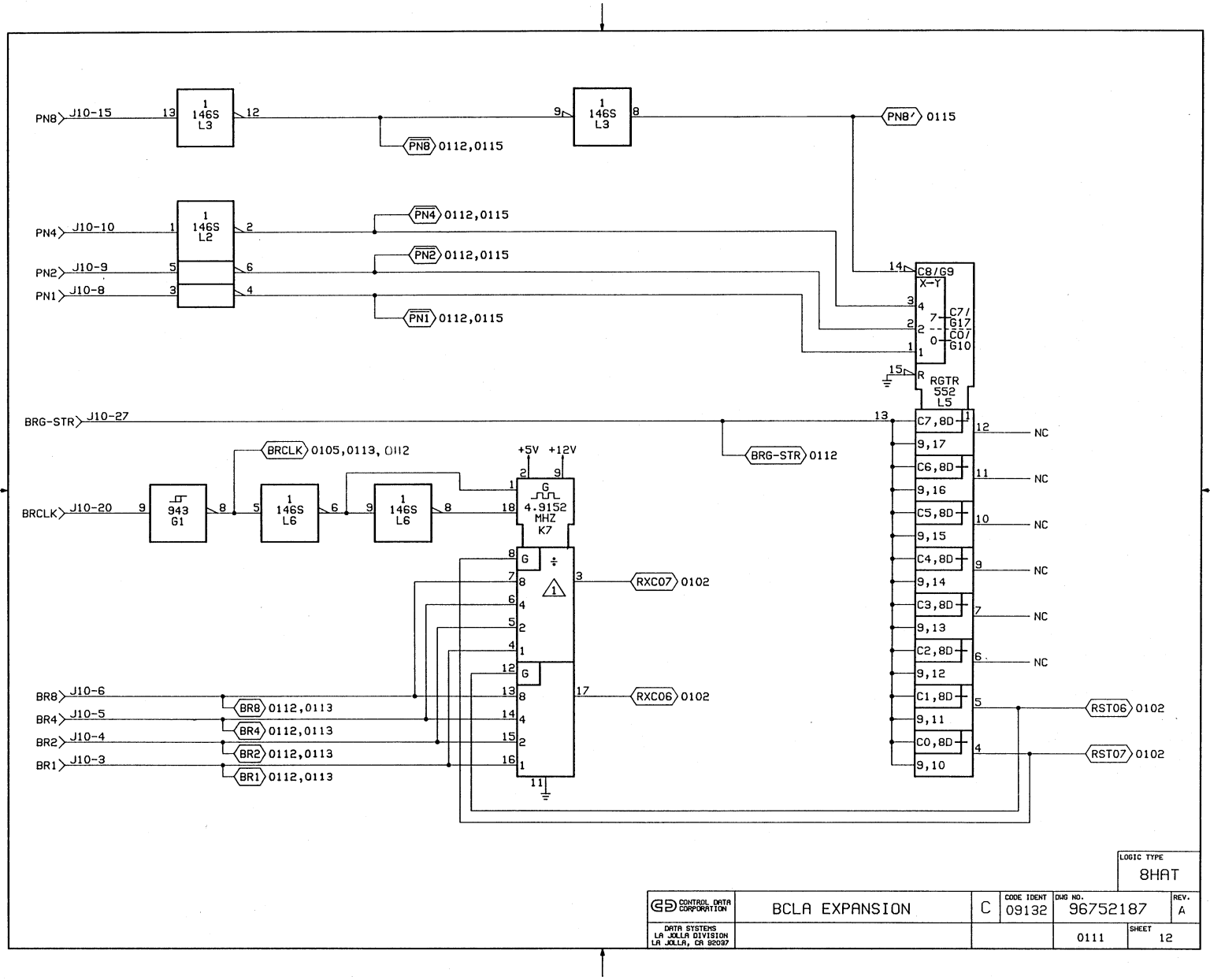


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 12 of 16)

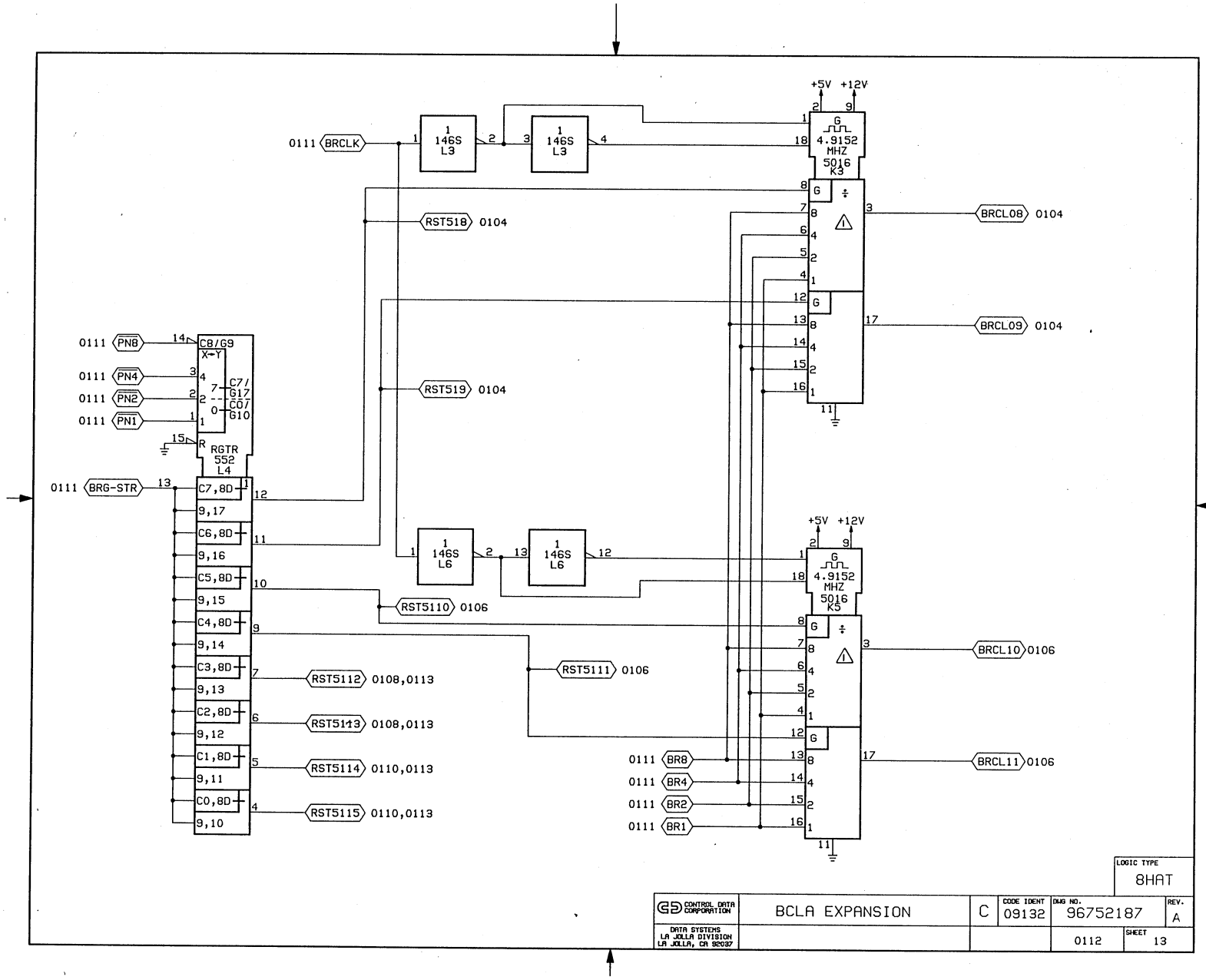


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 13 of 16)

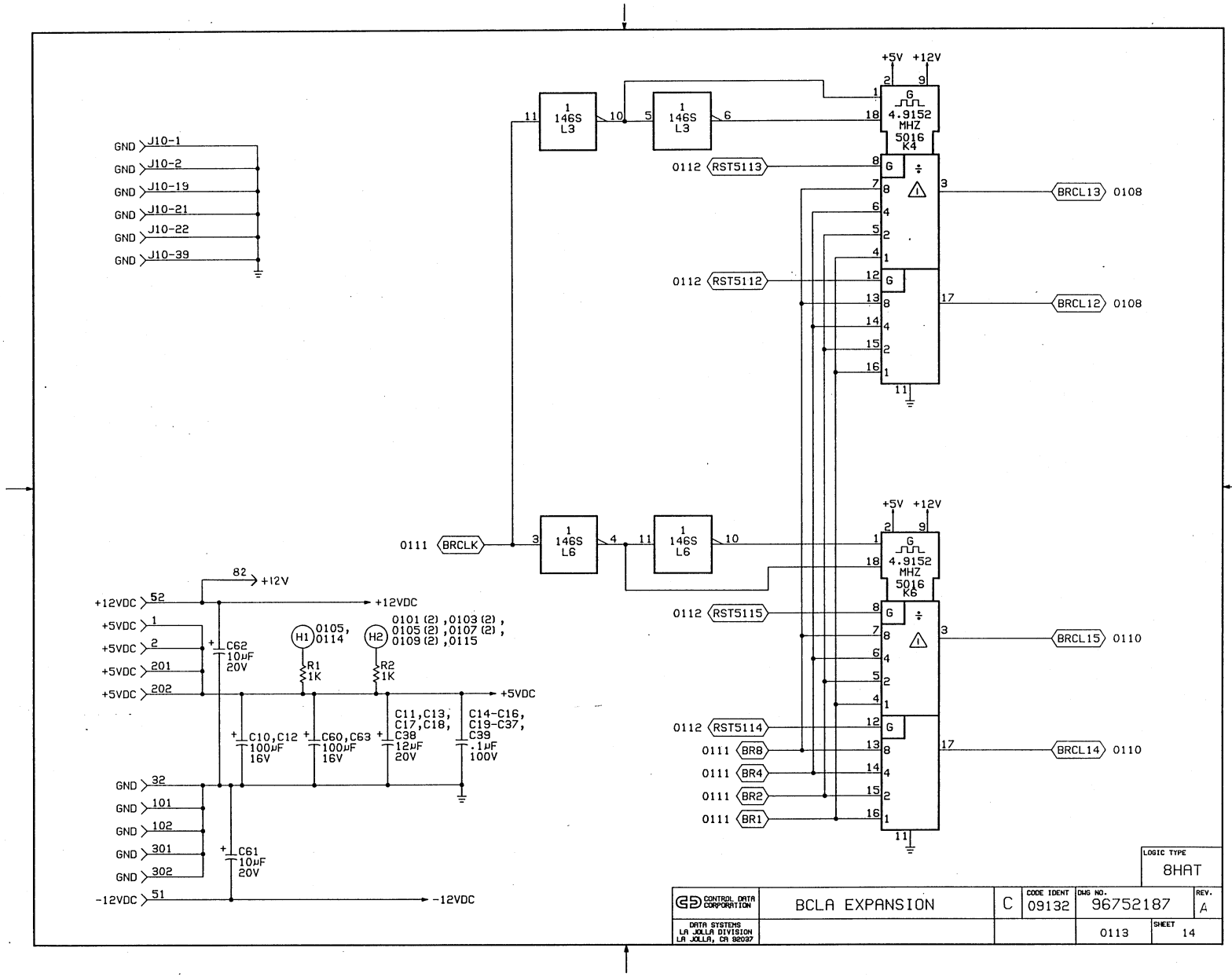


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 14 of 16)

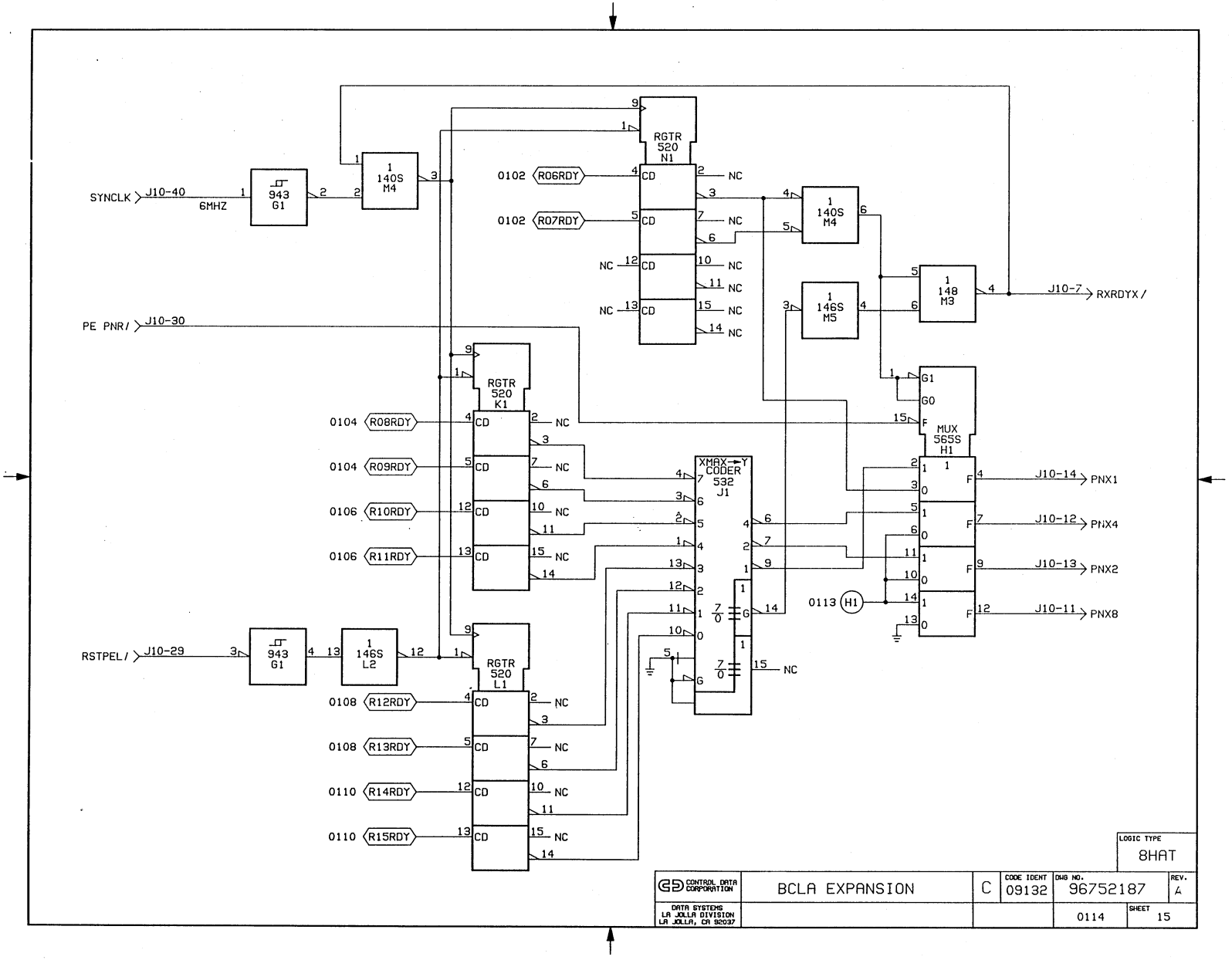


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 15 of 16)

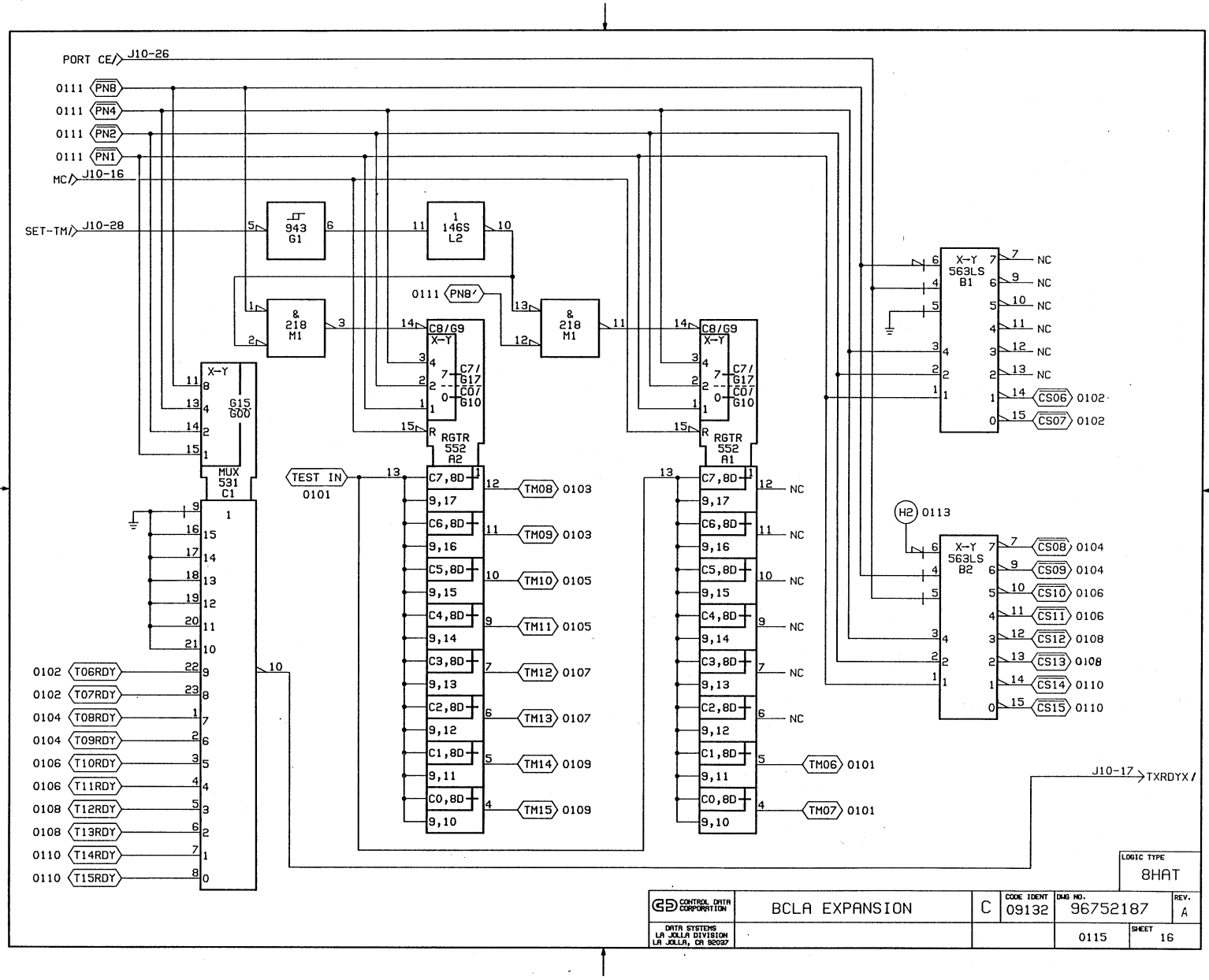


Figure 5-5. Expansion BCLA Logic Diagram (Sheet 16 of 16)

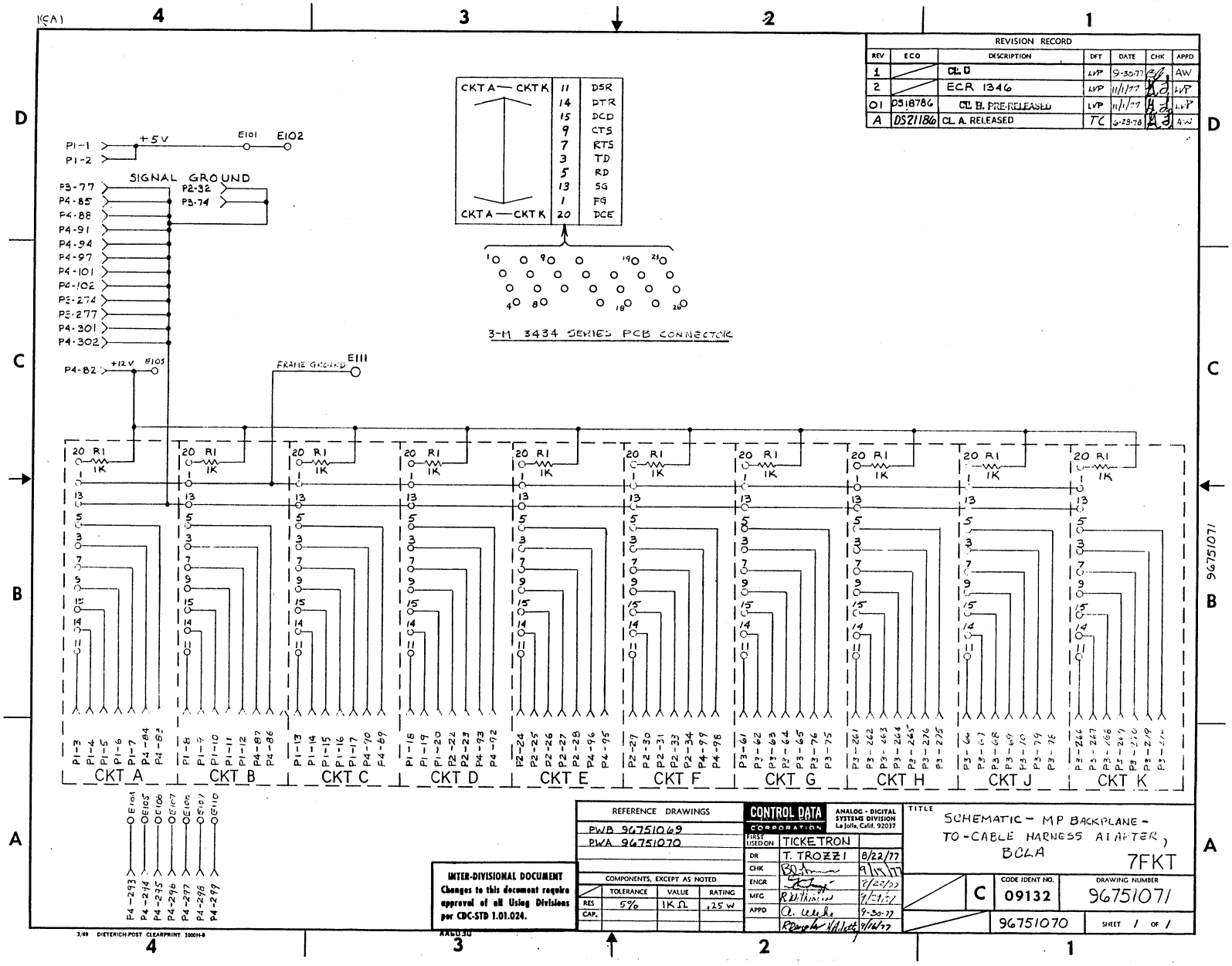
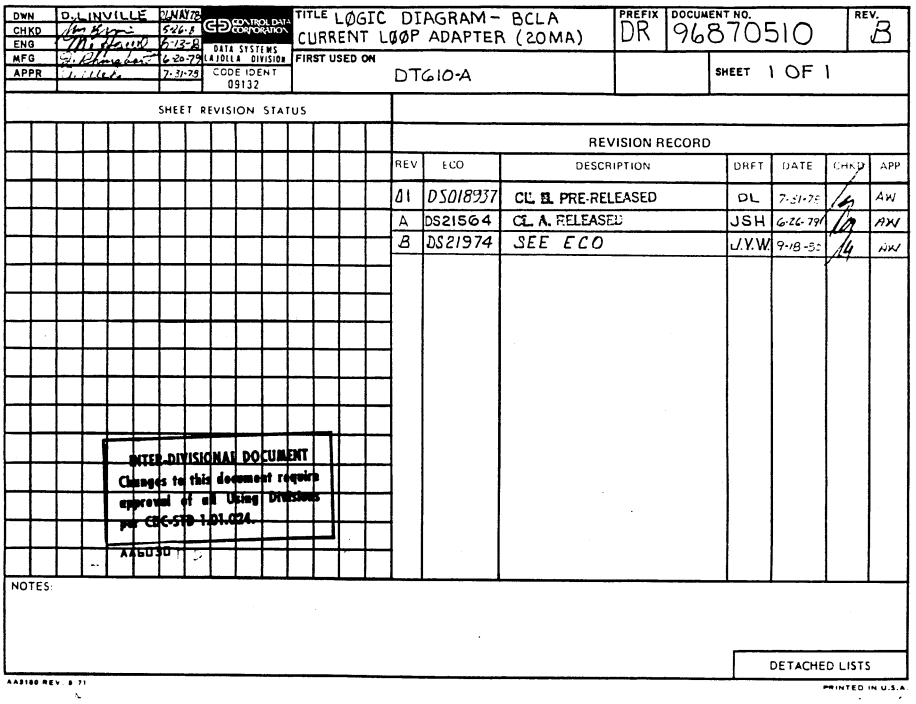


Figure 5-6. Expansion BCLA Cable Harness Adapter Schematic Diagram



DWN	D. LINVILLE	5/MAY/78	CONTROL DATA CORPORATION	TITLE LOGIC DIAGRAM - BCLA CURRENT LOOP ADAPTER (20MA)	PREFIX DR	DOCUMENT NO. 96870510	REV. B
CHKD		5-26-8					
ENG		6-13-8	DATA SYSTEMS LA JOLLA DIVISION	FIRST USED ON DT610-A		SHEET 1 OF 1	
MFG		6-20-79					
APPR		7-31-79	CODE IDENT 09132				

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	DS018937	CL B. PRE-RELEASED	DL	7-31-79		AW
A	DS21564	CL A. RELEASED	JSH	6-26-79		AW
B	DS21974	SEE ECO	J.Y.W.	9-18-80		AW

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD-1.01.024.

NOTES:

DETACHED LISTS

AA3180 REV. B 71

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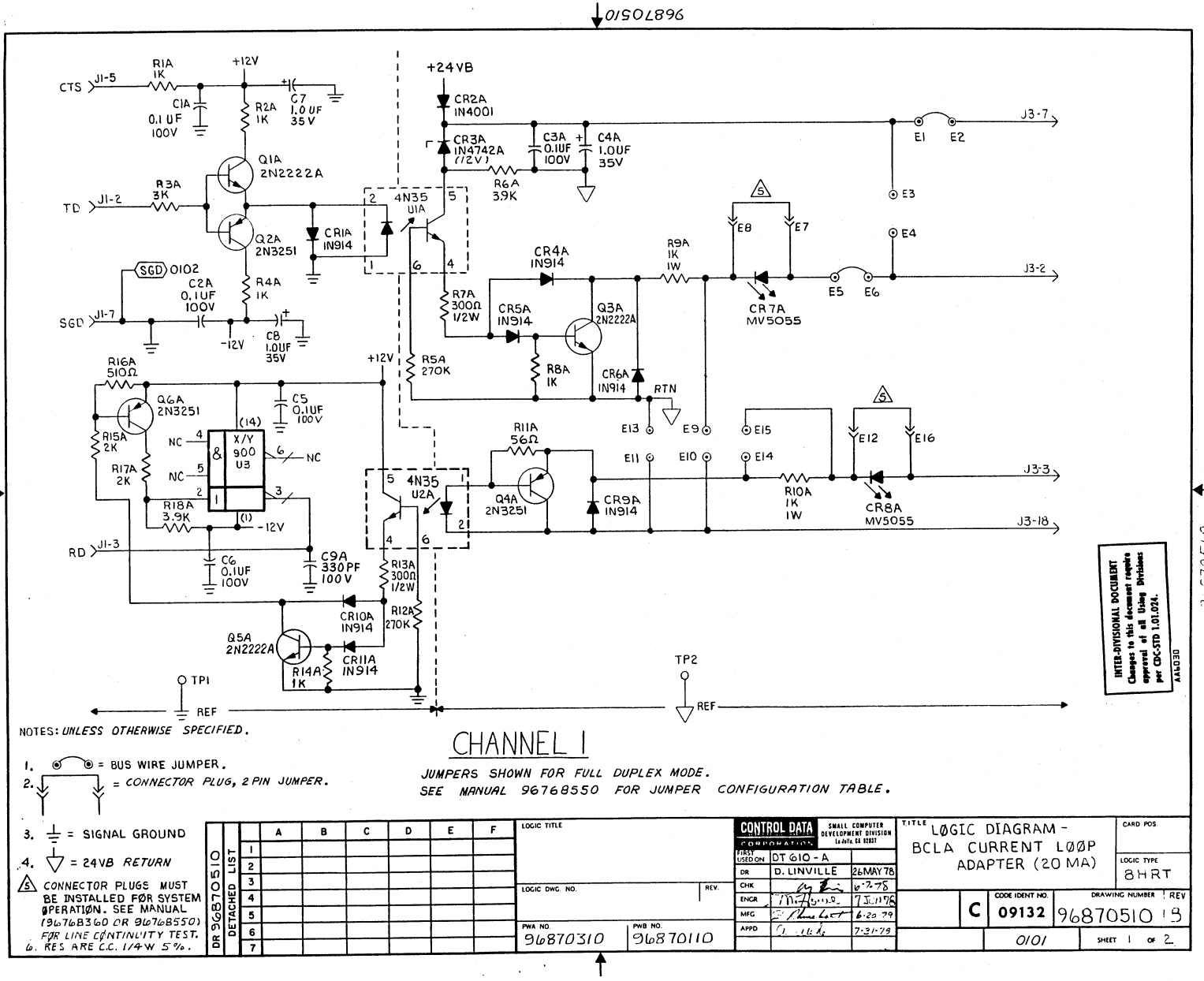
Figure 5-7. BCLA Current Loop Adapter Schematic Diagram (Sheet 1 of 3)



NOTES: *UNLESS OTHERWISE SPECIFIED.*

1. = BUS WIRE JUMPER.
2. = *CONNECTOR PLUG, 2 PIN JUMPER.*
3. = SIGNAL GROUND
4. = 24VB *RETURN*
5. CONNECTOR PLUGS MUST BE INSTALLED FØR SYSTEM ØPERATIØN. SEE MANUAL (96768360 OR 96768550) FØR LINE CONTINUITY TEST.
6. RES ARE C.C. 1/4W 5%.

CHANNEL 1

JUMPERS SHOWN FOR FULL DUPLEX MODE.
SEE MANUAL 96768550 FOR JUMPER CONFIGURATION TABLE.

DR 96870510 DETACHED LIST

	A	B	C	D	E	F
1						
2						
3						
4						
5						
6						
7						

LOGIC TITLE
LOGIC DWG. NO. REV.
PWA NO. 96870310 PWB NO. 96870110

CONTROL DATA CORPORATION — SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, CA 92037

FIRST USED ON	DT 610 - A	
DR	D. LINVILLE	26MAY78
CHK		6-7-78
ENGR		7-31-78
MFG		6-20-79
APPD		7-31-79

TITLE: LØGIC DIAGRAM - BCLA CURRENT LØØP ADAPTER (20 MA)

CARD POS.
LOGIC TYPE 8HRT

C | CODE IDENT NO. 09132 | DRAWING NUMBER 96870510 | REV 13

0101 | SHEET 1 OF 2

Figure 5-7. BCLA Current Loop Adapter Schematic Diagram (Sheet 2 of 3)

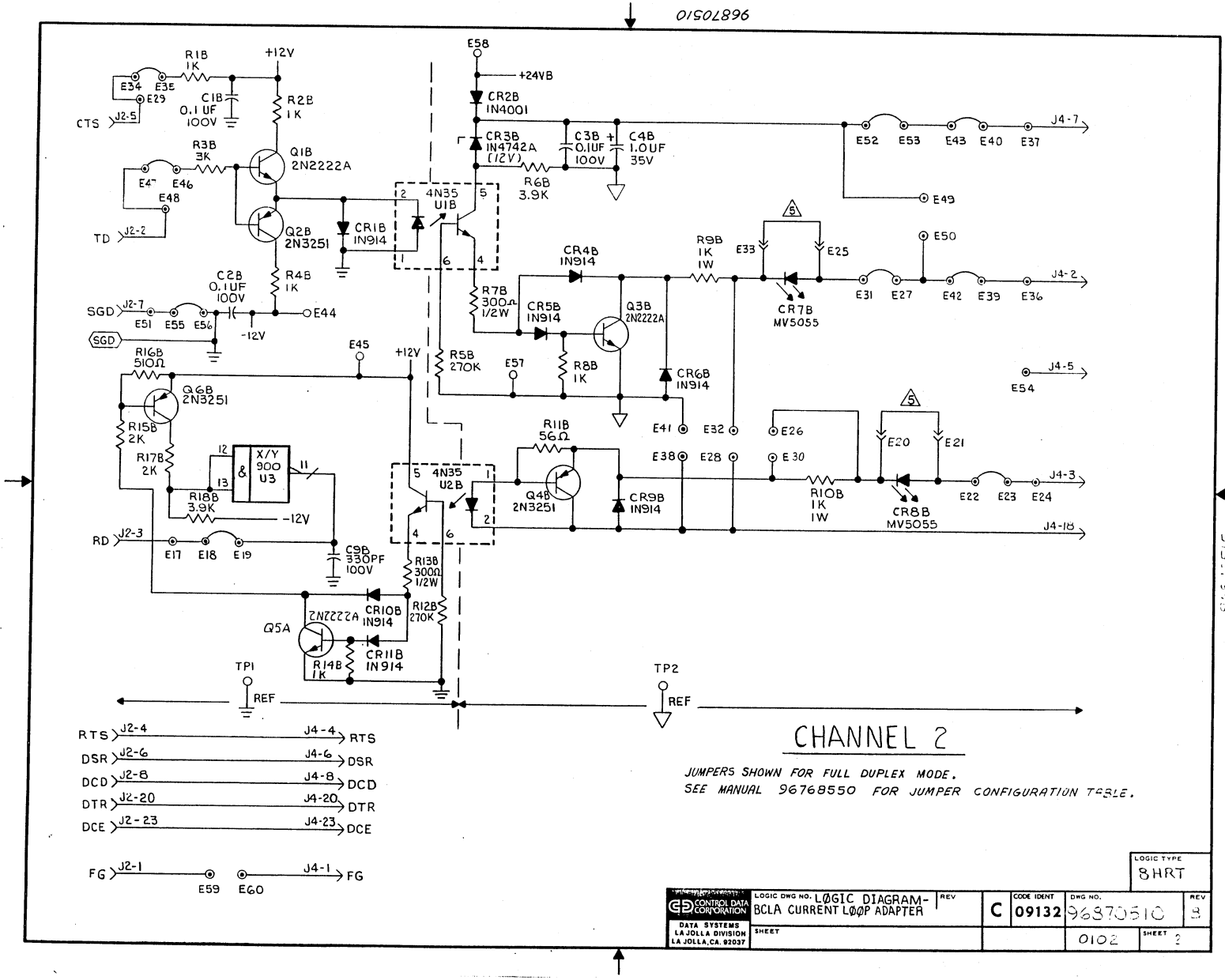


Figure 5-7. BCLA Current Loop Adapter Schematic Diagram (Sheet 3 of 3)

Onsite maintenance is limited to the diagnosis of a malfunction at the assembly level. Repair is effected by replacing the defective assembly with a previously tested spare. Refer to the associated subsystem hardware maintenance manual.

SPARES TESTING

All spare assemblies must be tested upon receipt and retested annually.

PREVENTIVE MAINTENANCE

No preventive maintenance is required for this equipment.

PARTS DATA 7

This section contains the following spare parts lists and assembly drawings with the parts listed:

(EA)

DWN		1-27-78	CONTROL DATA
CHKD		3-29-78	
ENG		5-27-78	DATA SYSTEMS LA JOLLA DIVISION
MFG		2/80	
APPR		3-29-78	CODE IDENT 09132
GS		4-28-78	

TITLE SPL - FJ127-A BCLA PRIMARY

PREFIX SPL | DOCUMENT NO. 96750692 | REV A

FIRST USED ON FJ127-A

SHEET 1 OF 2

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	ORFT	DATE	APP
01	DS18842	CL. B. PRE-RELEASED	JM	3-29-78	AW
02	DS21492	P/L CHG.	B.J.	4-30-79	AW
A	DS21748	CL. A. RELEASED	KDR	2-20-80	AW

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AA8030 C A

NOTES:

DETACHED LISTS

AA3100 REV. 8/71

PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH 2

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96750692	A	CLA	A	SPL-FJ127-A BCLA PRIMARY	DSM	FJ127A	03/29/78	02/09/80	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
2	A	96720419	100	PC	PWA-BCLA PRIMARY 9KLT	IN	021492	06 01 79	AYM4		N
4	A	96720730	100	PC	CABLE ASSY-PORT TO PORT TEST	IN	021492	06 01 79	AYM4		N
1	C	96751072	100	PC	PWA-BKPLN TO CABLE HARN (7FLT)	IN			AYM4		N
~~2~~	~~B~~	~~96752121~~	~~100~~	~~PC~~	~~PWA-BCLA PRIMARY SHDT~~	~~OUT~~	~~021492~~	~~06 01 79~~	~~AYM4~~		~~N~~
3	A	96752734	100	PC	JUMPER ASSEMBLY BCLA	IN			AYM4		N

NUMBER OF LINE ITEMS = 5
HIGHEST FIND NUMBER = 4

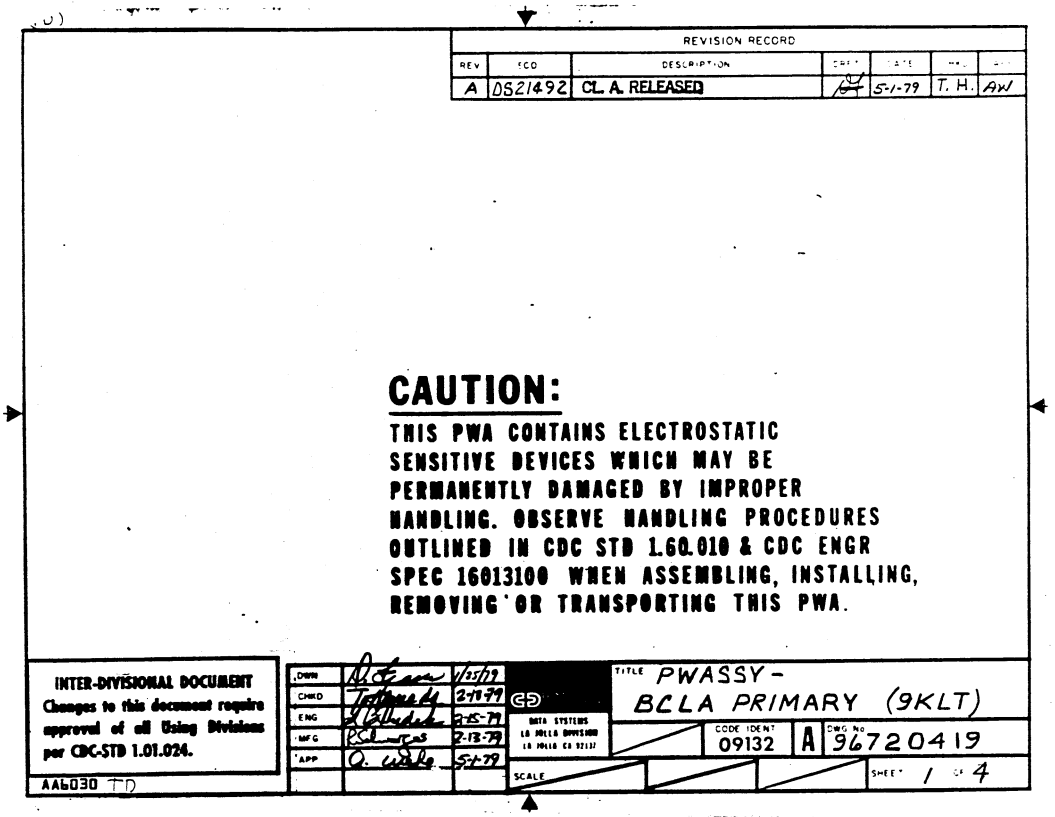
PROJECT ENGINEER

SCMD

INTERDIVISIONAL DOCUMENT

AA 2709-1 REV. 7-75

Figure 7-1. Primary BCLA Spare Parts List



REVISION RECORD						
REV	ECO	DESCRIPTION				
A	DS21492	CL. A. RELEASED		5-1-79	T. H.	AW

CAUTION:

THIS PWA CONTAINS ELECTROSTATIC SENSITIVE DEVICES WHICH MAY BE PERMANENTLY DAMAGED BY IMPROPER HANDLING. OBSERVE HANDLING PROCEDURES OUTLINED IN CDC STD 1.60.010 & CDC ENGR SPEC 16013100 WHEN ASSEMBLING, INSTALLING, REMOVING OR TRANSPORTING THIS PWA.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030 TD

DWN		1/25/79
CHKD		2-9-79
ENG		2-15-79
MFG		2-13-79
APP		5-1-79

CONTROL DATA CORPORATION
DATA SYSTEMS
LA JOLLA DIVISION
LA JOLLA CA 92037

TITLE PWASSY - BCLA PRIMARY (9KLT)

CODE IDENT 09132 | A | DWG NO 96720419

SCALE | SHEET 1 OF 4

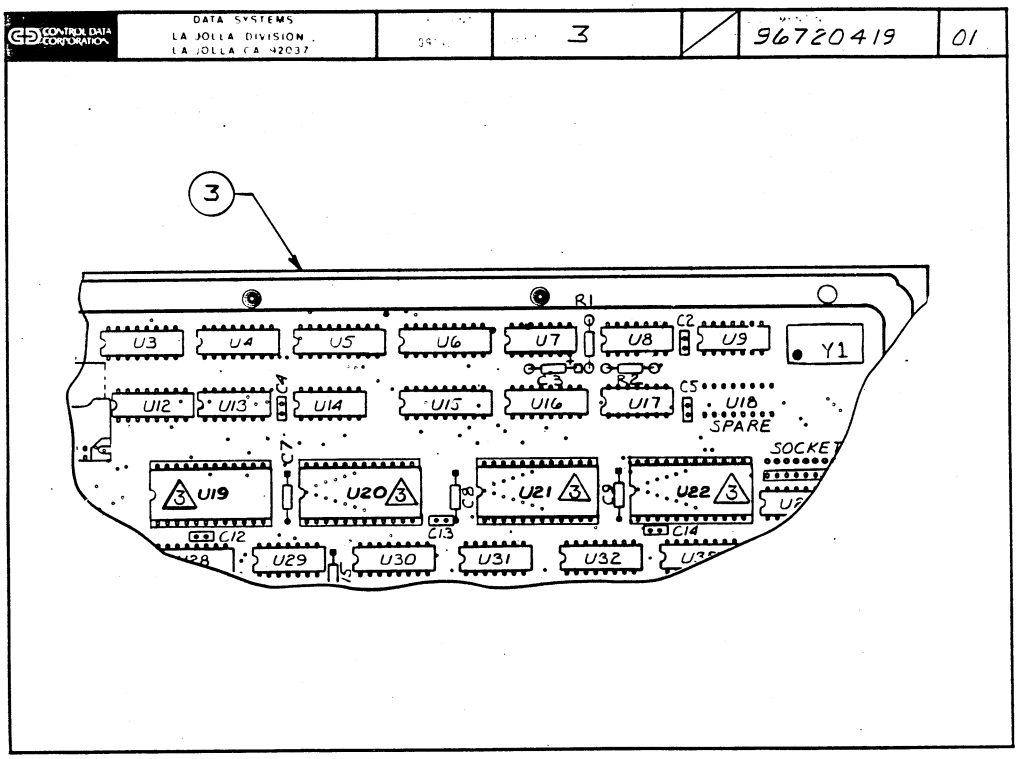
CONTROL DATA CORPORATION	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA CA 92037		Z		96720419	01

NOTES:

1. MARK PART NO. PER CDC SPEC 88818000.
2. WHEN PWA IS SOLD AS A SPARE FPP 96720420 MUST ACCOMPANY PWA.
3. INSTALL (F/N 2) ROM SET PER TABLE BELOW: INSURE I.C. PIN 1 MATCHES SOCKET PIN 1

ROM SET (SEE SH 3)	
PART NO.	LOCATION
96720724	U19 (BITS 00-07)
96720725	U20 (BITS 08-15)
96750265	U21 (BITS 16-23)
96720726	U22 (BITS 24-31)

Figure 7-2. Primary BCLA Printed Wiring Assembly (Sheet 1 of 2)



CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96720419	A	CLA	A	PWA-BCLA PRIMARY 9KLT	DS	CBR 18	04/21/79	04/21/79	1/1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
3	D	96720418	1.00	PC	PW SUBASSY-BCLA PRIMARY	IN					N
2	A	96720723	1.00	PC	ROM SET,BCLA	IN					N
1	C	96752198	REF	PC	LOGIC DIAG-BCLA PRI 8HDT/9KLT	IN			RFE4		N

NUMBER OF LINE ITEMS = 3
HIGHEST FIND NUMBER = 3

PROJECT ENGINEER

SCMD

AA 2709-1 REV. 7-75

Figure 7-2. Primary BCLA Printed Wiring Assembly (Sheet 2 of 2)

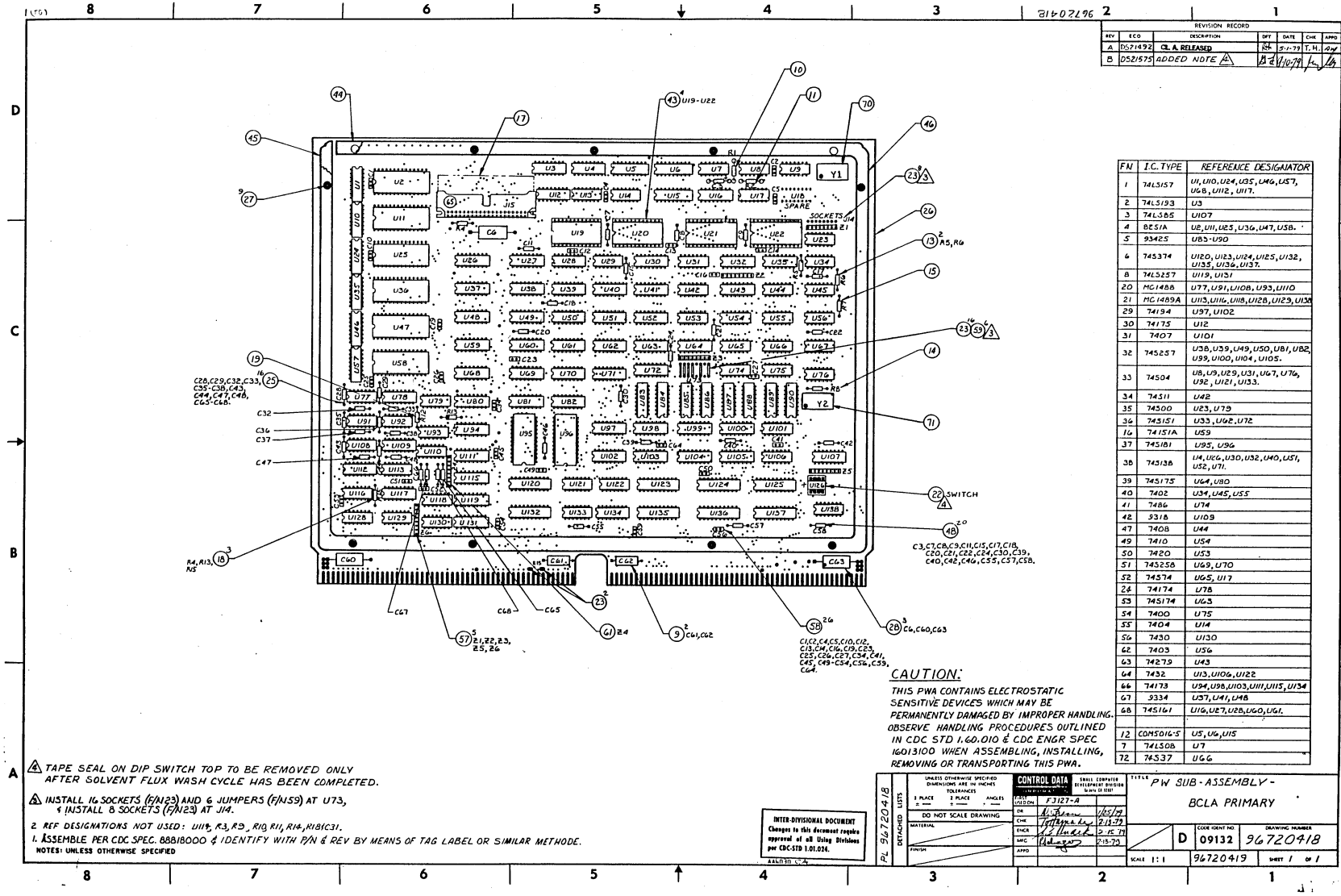


Figure 7-3. Primary BCLA Printed Wiring Sub-Assembly (Sheet 1 of 3)

DWN		2-13-79	CDC	TITLE PW SUB-ASSEMBLY - BCLA PRIMARY	PREFIX PL	DOCUMENT NO. 96720418	REV. B
CHKD		2-13-79					
ENG		2-15-79	DATA SYSTEMS LAJOLLA DIVISION				
MFG		2-13-79		FIRST USED ON FJ127-A		SHEET 1 OF 3	
APPR		2-15-79	CODE IDENT 09132				

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
A	DS21492	CL. A. RELEASED		5-1-79	T. H	
B	DS21575	F/N 22 WAS 39396502		9-05-79		

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD .01.024.

NOTES: AA6030 +

DETACHED LISTS

AA3186 REV. 6/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S SPARE PARTS
N NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	FAIL NUMBER
96720418	B	CLA	D	PW SUBASSY-BCLA PRIMARY	DSM	CAP 18	04/21/79	09/22/79	~~1/ 1~~

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	ON NC	ON CL
7	A	15145400	100	PC	IC TTL QUAD 2INPUT AND 74LS08	IN			PPP4		N
1	A	15146700	900	PC	IC MULTI•TTL QUAD 2 74LS157	IN			PPP4		N
2	A	15147000	100	PC	IC COUNTER TTL 4-BIT 74LS193	IN			PPP4		N
3	A	15147200	100	PC	IC-74LS85 TTL 4 BIT COMPARATOR	IN			PPP4		N
4	A	15155500	600	PC	IC 8251 SILICON GATE MOS	IN			PPP4		N
5	A	15155800	800	PC	IC-TTL RAM 1024x1 93425	IN			PPP4		N
12	A	15163219	300	PC	IC-COM5016-5 DUAL BAUD RT GEN	IN			PPP4		N
6	A	15163310	800	PC	IC 74S374 OCTAL LATCH TTL	IN			PPP4		N
72	A	15163312	100	PC	IC 74S37 QUAD NAND TTL	IN			PPP4		N
8	A	15164402	200	PC	IC 74LS257 MULTIPLEXER	IN			PPP4		N
10	C	17705905	100	PC	RES FXD .25W 51000 OHMS	IN			PPP4		N
11	C	17705912	100	PC	RES FXD .25W 0.1 MEG OHMS	IN			PPP4		N
9	C	17706766	200	PC	CAP FIXED SOLID TANTALUM 110	IN			PPP4		N
13	C	24500051	200	PC	RES FXD .25W 330 OHMS	IN			PPP4		N
14	C	24500053	100	PC	RES FXD .25W 390 OHMS	IN			PPP4		N
15	C	24500055	100	PC	RES FXD .25W 470 OHMS	IN			PPP4		N
18	C	24500063	300	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
19	C	24500087	100	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
20	A	36186400	500	PC	IC CHIP,TYPE 1488	IN			PPP4		N
21	A	36186501	500	PC	IC CHIP TYPE 1489	IN			PPP4		N
17	A	39122404	250	IN	TAPE-PLSTC FILM,ADH,1 IN. WIDE	IN			PPP3		N
~~22~~	~~A~~	~~39396502~~	~~100~~	~~PC~~	~~SWITCH, LOW PROFILE DIP-4PST 4 OUT~~	~~OUT~~	~~021575~~	~~0116A0~~	~~PPP4~~		~~N~~
23	A	39397400	2400	PC	SOCKET, MINIATURE SPRING	IN			PPP4		N
25	A	84996719	1600	PC	CAP,CER 100V 330 PF	IN			PPP4		N
27	A	88812400	900	PC	PIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
28	A	88880500	300	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
16	A	98881100	100	PC	IC 74151A TTL DATA SEL MUX	IN			PPP4		N
29	A	88881600	200	PC	IC 74194 TTL 4-BIT BIDIR S REG	IN			PPP4		N
24	A	88882800	100	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN			PPP4		N
30	A	88882900	100	PC	IC 74175 TTL QUAD D F/F W/CLR	IN			PPP4		N
31	A	88883200	100	PC	IC 7407 TTL HEX BUFFER (OC)	IN			PPP4		N
32	A	88883300	1000	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
33	A	88883700	900	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN			PPP4		N
34	A	88884100	100	PC	IC 74S11 SCHOTTKY TTL TPL 3-I	IN			PPP4		N
35	A	88884500	200	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN			PPP4		N
36	A	88884700	300	PC	IC-74S151 TTL DATA SELECTR/MUX	IN			PPP4		N

PROJECT ENGINEER

AA 2709-1 REV 7-75

SCMD

INTERDIVISIONAL DOCUMENT

Figure 7-3. Primary BCLA Printed Wiring Sub-Assembly (Sheet 2 of 3)

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96720418	B	CLA	D	PW SUBASSY-BCLA PRIMARY	DSM	C3R 18	04/21/79	08/22/79	2/ 3

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
37	A	88884900	2.00	PC	IC 74S181 TTL ALU/FUNCTION GEN	IN			PPP4		N
38	A	88885100	2.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N
39	A	88885200	3.00	PC	IC 74S175 TTL QUAD D F/F W/CLR	IN			PPP4		N
40	A	88885500	3.00	PC	IC 7402 TTL QUAD NOR GATE	IN			PPP4		N
41	A	88885700	1.00	PC	IC 74H6 TTL QUAD 2-IN EXCL OR	IN			PPP4		N
42	A	88886000	1.00	PC	IC 9318 TTL 8-IN PRIOR ENCODER	IN			PPP4		N
43	A	88889102	4.00	PC	SOCKET-IC 24 PIN,LOW PROFILE	IN			PPP4		N
44	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
45	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
46	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPP4		N
47	A	88897000	1.00	PC	IC 7408 TTL QUAD 2-INPUT AND	IN			PPP4		N
48	A	88897800	20.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
49	A	88898200	1.00	PC	IC 7410 TTL TRPL 3-IN POS NAND	IN			PPP4		N
50	A	88898400	1.00	PC	IC 7420 TTL DUAL 4-IN NAND	IN			PPP4		N
51	A	88920800	2.00	PC	IC 74S258 TTL QUAD 1-L SEL/MUX	IN			PPP4		N
52	A	88923000	2.00	PC	IC 74S74 TTL DUAL D EDGE F/F	IN			PPP4		N
53	A	88923100	1.00	PC	IC 74S174 TTL HEX D FLIP/FLOP	IN			PPP4		N
54	A	88924400	1.00	PC	IC 7400 TTL QUAD 2-I POS NAND	IN			PPP4		N
55	A	88924500	1.00	PC	IC 7404 TTL HEX INVERTER	IN			PPP4		N
56	A	88924600	1.00	PC	IC 7430 TTL QUAD 2-IN POS NAND	IN			PPP4		N
57	A	88924700	5.00	PC	RES NETWORK-SIP,8 PIN,1.K OHM	IN			PPP4		N
58	A	89636158	24.00	PC	CAP FXD CER .1MFD 100VDCW	IN			PPP4		N
59	A	89684100	6.00	PC	CONNECTOR PLUG TWO PIN JUMPER	IN			PPP4		N
61	A	94375105	1.00	PC	RES NETWORK, 8PIN SIP 10K OHMS	IN			PPP4		N
22	A	94398002	1.00	PC	SWITCH,SLIDE-DIP-PCB,4 POS	IN	021575	01184 80	PPP4		N
62	A	96744154	1.00	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN			PPP4		N
63	A	96744157	1.00	PC	IC 74279 TTL S-R LATCH	IN			PPP4		N
64	A	96744172	3.00	PC	IC 7432 TTL QUAD 2-IN OR GATE	IN			PPP4		N
65	A	96744934	1.00	PC	CONNECTOR,HEADER,RT ANGLE 2X20	IN			PPP4		N
66	A	96745300	6.00	PC	IC 74173 TTL TRI-ST QUAD D-F/F	IN			PPP4		N
67	A	96745400	3.00	PC	IC 9334 TTL 8-BIT ADDRES LATCH	IN			PPP4		N
68	A	96745500	5.00	PC	IC 74S161 TTL 4-BIT BINARY CTR	IN			PPP4		N
26	D	96752195	1.00	PC	PWB-BCLA PRIMARY	IN			PPP4		N
70	A	96760400	1.00	PC	OSCILLATOR-HRO CLK, 4.9152 MHZ	IN			PPP4		N
71	A	96760405	1.00	PC	OSCILLATOR-HRO CLK,12.0000 MHZ	IN			PPP4		N
					NUMBER OF LINE ITEMS = 71						

PROJECT ENGINEER

AA 2709-1 REV. 7-75

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Figure 7-3. Primary BCLA Printed Wiring Sub-Assembly (Sheet 3 of 3)

DWN	K.T. Peters	11/5/77	CONTROL DATA	TITLE PWA-MP BACKPLANE-TO-CABLE HARNESS ADAPTER, BCLA (7FLT)	PREFIX	DOCUMENT NO.	REV.
CHKD	[illegible]	12-20-77			PL	96751072	A
ENG	[illegible]	12-20-77	DATA SYSTEMS LAJOLLA DIVISION	FIRST USED ON FJ127-A		SHEET 1 OF 2	
MFG	[illegible]	11-4-77					
APPR	K.T. Peters	12/20/77	CODE IDENT 09132				

SHEET REVISION STATUS

REVISION RECORD					
REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	DS18800	CL. B. PRE-RELEASED	LWP	12/24/77	LWP
02	DS21286	SEE ECO	JSH	10-12-78	AW
03	DS15530	ADDED F/N 8 & 9	KB	11-27-79	AW
A	DS21748	CL. A. RELEASED	RJR	2-20-80	AW

INTER-DIVISIONAL DOCUMENT
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TD

NOTES:

DETACHED LISTS

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CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH 2

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96751072	A	CLA	C	PWA-BKPLN TO CABLE HARN (7FLT)	DSM	BCLA	12/17/77	02/09/80	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	EC NO.	S OR N
1	C	24500063	600	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
7	A	44670273	600	PC	CONN-SOLDER PCB 26 CONTACTS	IN	021286	092278	PPP4		N
2	C	75743607	100	PC	HEADER-RIGHT ANGLE (7 PIN)	IN	021286	092278	PPP4		N
~~2~~	~~A~~	~~80775001~~	~~700~~	~~PC~~	~~TERM,PIN-WIRE WRAP~~	~~OUT~~	~~021286~~	~~092278~~	~~PPP4~~		~~N~~
3	C	96751069	100	PC	PWB-BKPLN TO CABLE HARNESS	IN			PPP4		N
4	C	96751073	REF	PC	SCHEMATIC-BKPLN TO HARN (7FLT)	IN			RFE4		N
5	C	96752010	600	PC	CABLE ASSY RIBBON-25 POS 4 FT	IN			PPP4		N
6	A	96756701	300	PC	CONNECTOR-PWB .125 CENTERS	IN			PPP4		N
8	A	96837812	275	IN	TAPE-PLASTIC FILM,ADH, 1.0 W	IN	015530	111379	PPP3		N
9	A	96837925	1425	IN	TAPE-ABRASN RESISTANT ADH 2.5W	IN	015530	111379	PPP4		N

NUMBER OF LINE ITEMS = 10
HIGHEST FIND NUMBER = 9

PROJECT ENGINEER

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INTERDIVISIONAL DOCUMENT

AA 2709-1 REV. 7-75

Figure 7-4. Primary BCLA Backplane-to-Cable-Harness PWA (Sheet 1 of 2)

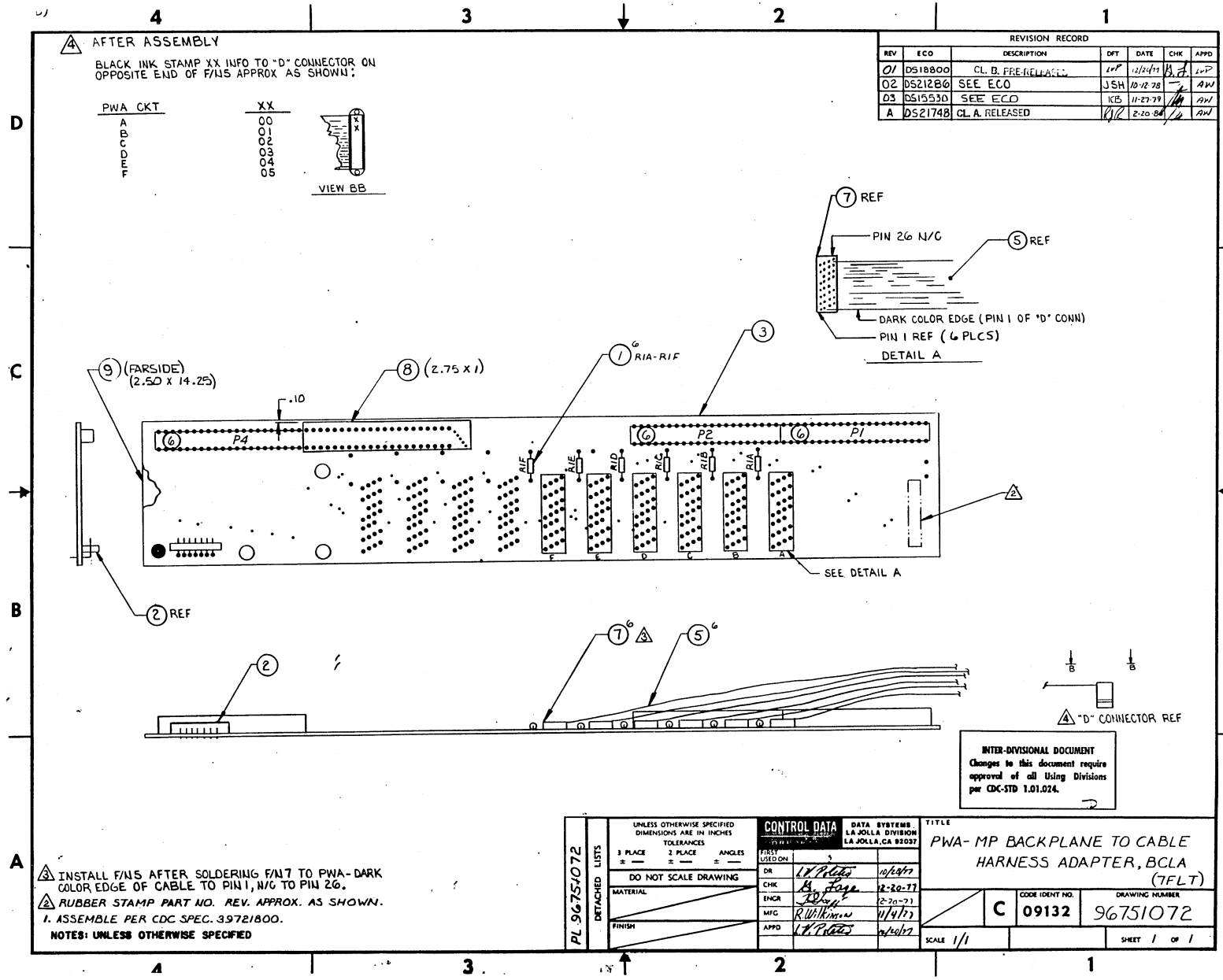


Figure 7-4. Primary BCLA Backplane-to-Cable-Harness PWA (Sheet 2 of 2)

TABULATION		
PART NO.	LENGTH	TOL. ⚠
96752007	1.00 FT	
96752008	2.00 FT	
96752009	3.00 FT	
96752010	4.00 FT	
96752011	5.00 FT	
96752012	6.00 FT	
96752013	7.00 FT	
96752014	8.00 FT	
96752015	9.00 FT	
96752016	10.00 FT	

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
01	D618797	CL. B. PRELEASED	[illegible]	1-25-78	[illegible]	AW
A	D521564	CL. A. RELEASED	JSH	6-26-78	[illegible]	AW

REQUIREMENTS:

⚠ MATERIAL & FINISH: BOARD CONNECTOR - GLASS REINFORCED THERMOPLASTIC RATED 94VEO (BLUE); CONTACTS OF BERYLLIUM COPPER, PLATED WITH BRIGHT ACID TIN OVER NICKEL. "D" CONNECTOR - GLASS REINFORCED THERMOPLASTIC RATED 94VEO (BLUE); CONTACTS OF BERYLLIUM COPPER PLATED WITH 30U IN. GOLD OVER NICKEL. CABLE - PVC (LIGHT BLUE) INSULATION RATED FR-1, 28AWG STRANDED COPPER, 25 POSITION .050 (1.27MM) SPACING.

2. OPERATING TEMPERATURE: BOARD CONNECTOR - -25°C TO 105°C. "D" CONNECTOR - -55°C TO 105°C. CABLE - -20° TO 105°C.

3. ELECTRICAL CHARACTERISTICS: BOARD CONNECTOR - CURRENT RATING IS 1 AMP, INSULATION RESISTANCE 1X10⁹ OHMS, DIELECTRIC STRENGTH IS 500 VDC AT SEA LEVEL. "D" CONNECTOR - CURRENT RATING 3 AMPS, INSULATION RESISTANCE IS GREATER THAN 1X10⁹ OHMS, DIELECTRIC STRENGTH IS GREATER THAN 500 VDC AT SEA LEVEL. CABLE - IMPEDANCE 105 OHMS, CAPACITANCE 15PF/FT (49PF/m), INDUCTANCE 0.20 UH/FT (0.66 UH/M), PROPAGATION DELAY IS 1.42 NS/FT (4.66 NS/m), INSULATION RESISTANCE IS GREATER THAN 10^{10} OHMS/10FT (3m), VOLTAGE RATING 300 V (RMS).

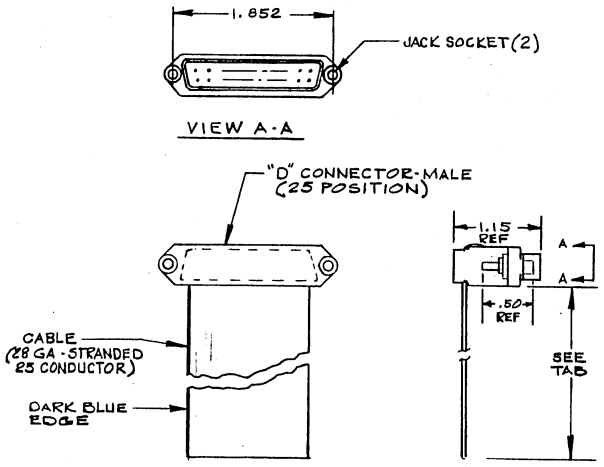
4. MARKING: PART SHALL BE PERMANENTLY AND LEGIBLY MARKED WITH MFG NAME OR SYMBOL.

5. IDENTIFICATION: IDENTIFY WITH CDC PART NO. & REV. LTR. TO WHICH THE PART IS MANUFACTURED, USING A TAG, LABEL OR SIMILAR METHOD PERMANENTLY ATTACHED.

6. MANUFACTURER:
"D" CONNECTOR - T&B ANSLEY (#609-25F),
CABLE - 3M (#3507/25), T&B ANSLEY (#171-50),
JACK SOCKET - T&B ANSLEY (#609-003) OR EQUIVALENT

⚠ TOLERANCE ON LENGTH $+1\%\ {}^{+.06}_{-.0}$

8. SOURCE: SEE QVL.



NOTES: UNLESS OTHERWISE SPECIFIED

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DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
3 PLACE ±.010 | 2 PLACE ±.03⚠ | ANGLES ± 1°
DO NOT SCALE DRAWING
MATERIAL ⚠
FINISH ⚠

CONTROL DATA CORPORATION — DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037

FIRST USED ON	CYBER 18	
DR	[illegible]	10 4 77
CHK	[illegible]	1-25-78
ENGR	[illegible]	1-25-78
MFG	R. Wilkin	11-14-77
APPD	[illegible]	1-25-78

SPEC CONTROL DWG

TITLE: CABLE ASSY, RIBBON - 25 POSITION, MALE "D" CONN.

SIZE	CODE IDENT NO.	DRAWING NUMBER
C	09132	96752007/16

SCALE | SHEET 1 OF 1

AA6030

Figure 7-5. 25-Position Flat Ribbon Cable

(TD)

DWN		1-30-78	CONTROL DATA
CHKD		3-29-78	
ENG		5-17-78	DATA SYSTEMS LA JOLLA DIVISION
MFG		6-20-78	
APPR		3-29-78	CODE IDENT 09132
ES		7-28-78	

TITLE SPL - FJ128-A, BCLA EXPANSION

FIRST USED ON FJ128-A

PREFIX	DOCUMENT NO.	REV.
SPL	96750696	A

SHEET 1 OF 2

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	DS18842	CL. B. PRE-RELEASED	JM	3-29-78	AW
A	DS21564	CL. A. RELEASED	JSH	6-29-79	AW

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AA6080 TD

NOTES:

DETACHED LISTS

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CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH. 2
MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96750696	A	CLA	A	SPL-FJ128-A BCLA EXPANSION	DSM	FJ128A	03/29/78	06/19/79	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	C	96751070	100	PC	PWA-BKPLN TO CABLE HARN (7FKT)	IN			AYM4		N
2	C	96751978	100	PC	CABLE ASSY-RIBBON,40 POS,4IN,F	IN			PPP4		N
3	C	96751990	100	PC	CABLE ASSY-RIBBON,40 POS, 16IN	IN			PPP4		N
4	D	96752186	100	PC	PWA-BCLA EXPANSION BHAT	IN			AYM4		N

NUMBER OF LINE ITEMS = 4
HIGHEST FIND NUMBER = 4

PROJECT ENGINEER

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AA 2708-1 REV. 7-75

Figure 7-6. Expansion BCLA Spare Parts List

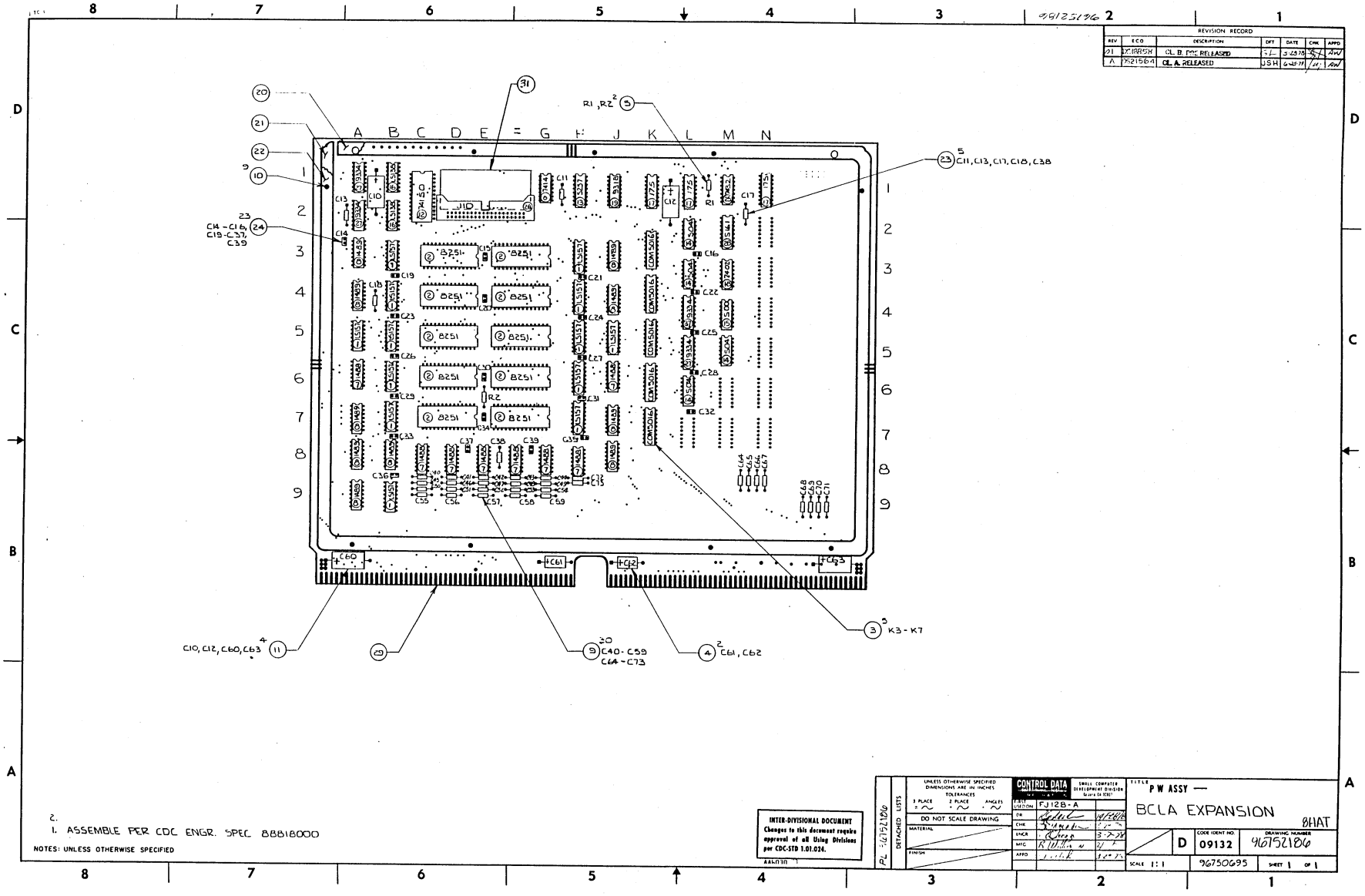

Figure 7-7. Expansion BCLA Printed Wiring Assembly (Sheet 1 of 2)

DWN	REINHARD JOHNSON	3-28-78	CONTROL DATA	TITLE PWA BCLA EXPANSION (8HAT)	PREFIX PL	DOCUMENT NO. 96752186	REV. A
CHKD		3-27-78					
ENG		3/27/78	DATA SYSTEMS LAJOLLA DIVISION	FIRST USED ON FJ128-A		SHEET 1 OF 2	
MFG		3-28-78	CODE IDENT 09132				
APPR		3-28-78					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	DS18858	CL B. PRE-RELEASED	RJ.	3-23-78	AW
A	DS21564	CL A. RELEASED	JSH	6-26-79	AW

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AA6030T D

NOTES:

DETACHED LISTS

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CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH.2
4F

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96752186	A	CLA	D	PWA-BCLA EXPANSION 8HAT	DSM	CRR 16	03/15/78	06/16/79	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PR NC	S OR N
1	A	15146700	1300	PC	IC MULTI,TTL QUAD 2 74LS157	IN			PPP4		N
16	A	15147400	200	PC	IC, DECODER-STTL 74LS138	IN			PPP4		N
2	A	15155500	1000	PC	IC 8251 SILICON GATE MOS	IN			PPP4		N
3	A	15163219	500	PC	IC-COM5016-5 DUAL BAUD RT GEN	IN			PPP4		N
4	C	17706766	200	PC	CAP FIXED SOLID TANTALUM 110	IN			PPP4		N
5	C	24500063	200	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
7	A	36186400	800	PC	IC CHIP,TYPE 1488	IN			PPP4		N
8	A	36186501	1000	PC	IC CHIP TYPE 1489	IN			PPP4		N
31	A	39122404	300	IN	TAPE-PLSTC FILM,ADH,1 IN. WIDE	IN	018858	031578	PPP3		N
9	A	84996719	3000	PC	CAP,CER 100V 330 PF	IN			PPP4		N
10	A	88812400	900	PC	RIVET-SEMI-TURULAR,BRS .312 LG	IN			PPP4		N
11	A	88880500	400	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
12	A	88881300	100	PC	IC 74150 TTL 16-BIT SEL/MUX	IN			PPP4		N
17	A	88882900	300	PC	IC 74175 TTL QUAD D F/F W/CLR	IN			PPP4		N
13	A	88883300	100	PC	IC 74S257 QUAD 2-L D SEL/MUX	IN			PPP4		N
14	A	88883700	400	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN			PPP4		N
15	A	88884500	100	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN			PPP4		N
18	A	88885500	100	PC	IC 7402 TTL QUAD NOR GATE	IN			PPP4		N
19	A	88886000	100	PC	IC 9318 TTL 8-IN PRIOR ENCODER	IN			PPP4		N
6	A	88896100	100	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN			PPP4		N
20	C	88896600	100	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
21	C	88896700	100	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
22	C	88896800	100	PC	FRAME-CARD (CASTING)	IN			PPP4		N
23	A	88897800	500	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
24	A	89636158	2300	PC	CAP FXD CER .1MFD 100VDCW	IN			PPP4		N
25	A	96744172	100	PC	IC 7432 TTL QUAD 2-IN OR GATE	IN			PPP4		N
26	A	96744934	100	PC	CONNECTOR,HEADER,RT ANGLE 2X20	IN			PPP4		N
27	A	96745400	400	PC	IC 9334 TTL 8-BIT ADDRES LATCH	IN			PPP4		N
28	A	96745500	100	PC	IC 74S161 TTL 4-BIT BINARY CTR	IN			PPP4		N
29	C	96752185	100	PC	PWB-BCLA EXPANSION	IN			PPP4		N
30	C	96752187	REF	PC	LOGIC-BCLA EXPANSION 8HAT	IN			PFE4		N
					NUMBER OF LINE ITEMS = 31						
					HIGHEST FIND NUMBER = 31						

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Figure 7-7. Expansion BCLA Printed Wiring Assembly (Sheet 2 of 2)

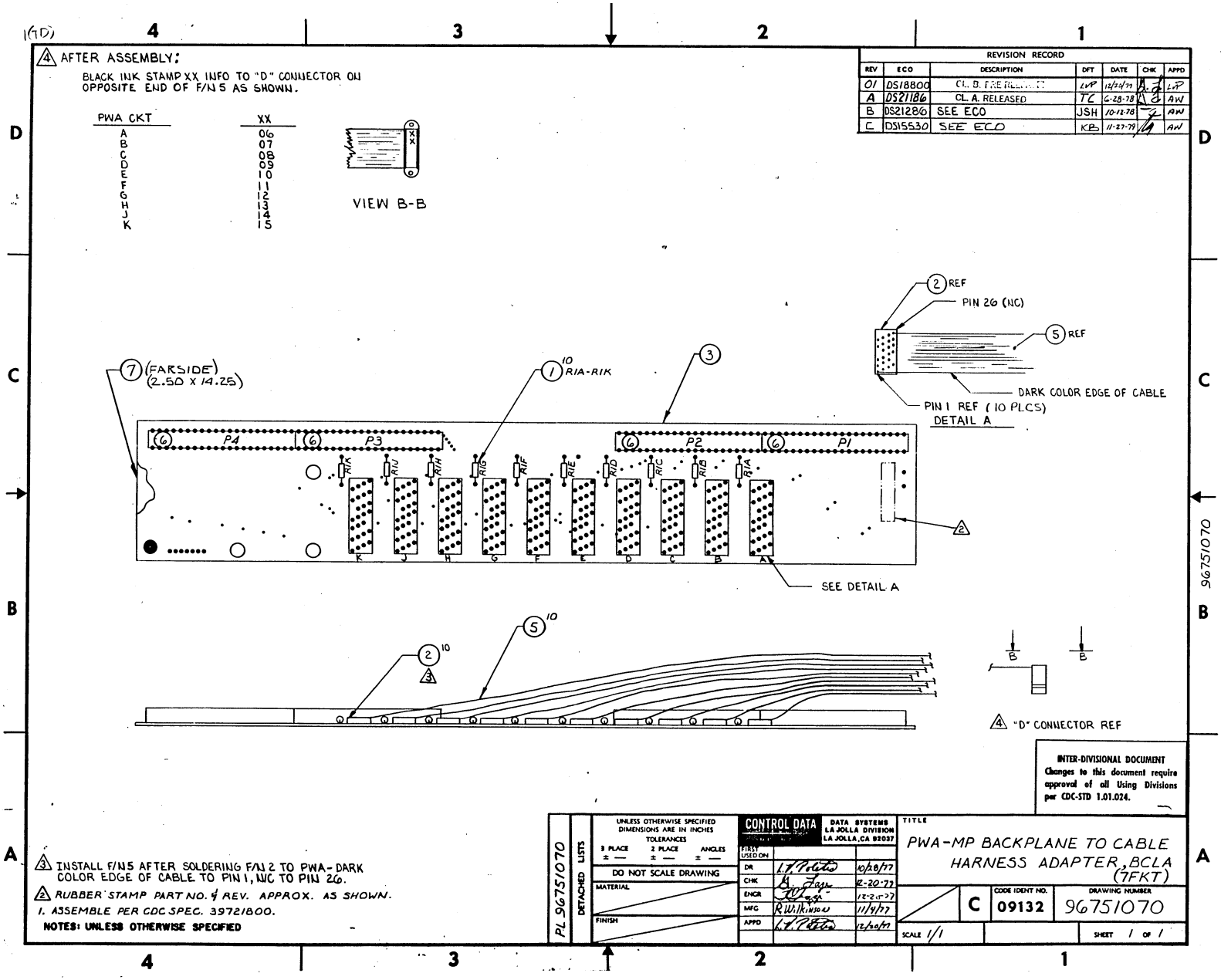

Figure 7-8. Expansion BCLA Backplane-to-Cable-Harness PWA (Sheet 1 of 2)

(110)

DWN		11/15/77	CONTROL DATA
CHKD		12-20-77	
ENG		12-20-77	DATA SYSTEMS LA JOLLA DIVISION
MFG		11/16/77	
APPR		12/20/77	CODE IDENT 09132

TITLE PWA-MP BACKPLANE-TO-CABLE HARNESS ADAPTER, BCLA (7FKT)

FIRST USED ON

PREFIX	DOCUMENT NO.	REV.
PL	96751070	C

SHEET 1 OF 2

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	DS18800	CL. B. PRE-RELEASED	LVP	12/22/77	LVP
A	DS21186	CL. A. RELEASED	TC	6-28-78	AW
B	DS21286	ADDED F/N 2	JSH	10-13-78	AW
C	DS15530	ADDED F/N 7	KB	11-27-79	AW

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AA4030

NOTES:

DETACHED LISTS

AA3180 REV. 8/71

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CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SHT. 2

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96751070	C	CLA	C	PWA-BKPLN TO CABLE HARN (7FKT)	DSM	TICKET	12/17/77	11/14/79	~~1/1~~

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	A OR N
1	C	24500063	1000	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
2	A	44670273	1000	PC	CONN-SOLDER PCB 26 CONTACTS	IN	021286	092278	PPP4		N
3	C	96751069	100	PC	PWB-BKPLN TO CABLE HARNESS	IN			PPP4		N
4	C	96751071	REF	PC	SCHEMATIC-BKPLN TO HARN (7FKT)	IN			RFE4		N
5	C	96752010	1000	PC	CABLE ASSY RIBBON-25 POS 4 FT	IN			PPP4		N
6	A	96756701	400	PC	CONNECTOR-PWB .125 CENTERS	IN			PPP4		N
7	A	96837925	1425	IN	TAPE-ABRASN RESISTANT ADH 2.5W	IN	015530	111379			N

NUMBER OF LINE ITEMS = 7
HIGHEST FIND NUMBER = 7

PROJECT ENGINEER

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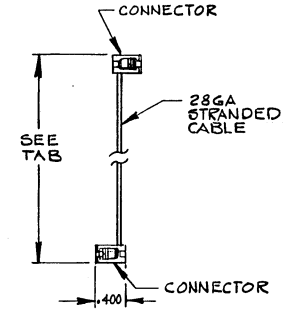
INTERDIVISIONAL DOCUMENT

AA 2709-1 REV. 7-75

Figure 7-8. Expansion BCLA Backplane-to-Cable-Harness PWA (Sheet 2 of 2)

TABULATION	
PART NO.	LENGTH ⚠1
96751975	1.00 IN
96751976	2.00 IN
96751977	3.00 IN
96751978	4.00 IN
96751979	5.00 IN
96751980	6.00 IN
96751981	7.00 IN
96751982	8.00 IN
96751983	9.00 IN
96751984	10.00 IN
96751985	11.00 IN
96751986	12.00 IN
96751987	13.00 IN
96751988	14.00 IN
96751989	15.00 IN
96751990	16.00 IN
96751991	17.00 IN
96751992	18.00 IN
96751993	19.00 IN
96751994	20.00 IN



TERMINATED CONNECTOR
NOTE ORIENTATION OF CONNECTORS.

REQUIREMENTS:

⚠1 MATERIAL & FINISH: GLASS FILLED THERMO PLASTIC (BLUE); CONTACTS MADE OF BERYLLIUM COPPER, .00003IN. GOLD PLATING OVER NICKEL; FLAMMABILITY IS UL RATED 96 VEO; CABLE IS INSULATED WITH PVC.

2. OPERATING TEMPERATURE: -55°C TO 105°C.

3. ELECTRICAL CHARACTERISTICS: CURRENT RATING IS 1 AMP; DIELECTRIC STRENGTH IS 500 V DC (SEA LEVEL).

4. MARKING: PART SHALL BE PERMANENTLY AND LEGIBLY MARKED WITH MFG. NAME OR SYMBOL.

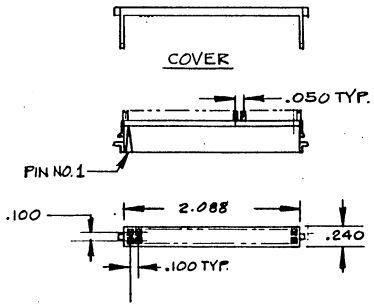
5. IDENTIFICATION: IDENTIFY WITH CDC PART NO. & REV LTR TO WHICH THE PART IS MANUFACTURED, USING A TAG, LABEL OR SIMILAR METHOD PERMANENTLY ATTACHED.

6. MANUFACTURER: T&B/ANSLEY CORP., "BLUE MAC8" CABLE/CONNECTOR SYSTEM; CONNECTOR: #609-4000 M. CABLE: #171-40.

⚠2 TOLERANCE ON LENGTH: $^{+1\%+.06}_{-.00}$ IN.

8. SOURCE: SEE QVL.

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
01	DS18797	CL. B. PRE-RELEASED	WCJ	1-25-78		DW
A	DS21564	CL. A. RELEASED	JSH	6-26-79		DW



CABLE
28 GA. STRANDED

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AAL030

NOTES: UNLESS OTHERWISE SPECIFIED

SPEC CONTROL DWG

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
3 PLACE ±.010 | 2 PLACE ±.03 ⚠1 | ANGLES ±1
DO NOT SCALE DRAWING
MATERIAL ⚠1
FINISH ⚠1

CONTROL DATA CORPORATION — DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037

FIRST USED ON		
DR		10-3-77
CHK		1-25-78
ENGR		1-25-78
MFG		11-14-77
APPD		1-25-78

DETACHED LISTS

TITLE
CABLE ASSY, RIBBON-40 POSITION, FEMALE

CODE IDENT NO.	DRAWING NUMBER
09132	96751975/96

C

SCALE

SHEET 1 OF 1

96751975/96

Figure 7-9. 40-Position Flat Ribbon Cable

DWN	[signature]	7-1-78	CONTROL DATA CORPORATION	TITLE SPL - DT610-A, CURRENT LOOP ADAPTER	PREFIX SPL	DOCUMENT NO. 96837754	REV. A
CHKD	[signature]	10.4.78					
ENG	[signature]	10-2-78	DATA SYSTEMS LA JOLLA DIVISION	FIRST USED ON DT610-A (1843)		SHEET 1 OF 2	
MFG	[signature]	6-20-79					
APPR	[signature]	10-5-78	CODE IDENT 09132				
	[signature]	10-4-78					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	DS18945	CL. B. PRE-RELEASED	JM	10-5-78	[illegible]	AWJ
A	DS21564	CL. A. RELEASED	JSH	6-25-79	[illegible]	AWJ

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AA6030 TS

NOTES:

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CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH. 2
MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96837754	A	CLA	A	SPL-DT610-A CURRENT LOOP ADAPT	DS	DT610A	10/03/78	06/16/79	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE GRD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	C	96870310	100	PC	PWA-BCLA CUR LOOP ADPTR 8HRT	IN			AY44		N

NUMBER OF LINE ITEMS = 1
HIGHEST FIND NUMBER = 1

PROJECT ENGINEER

SCMD

AA 2708-1 REV. 7-75

Figure 7-10. Current Loop Adapter Spare Parts List

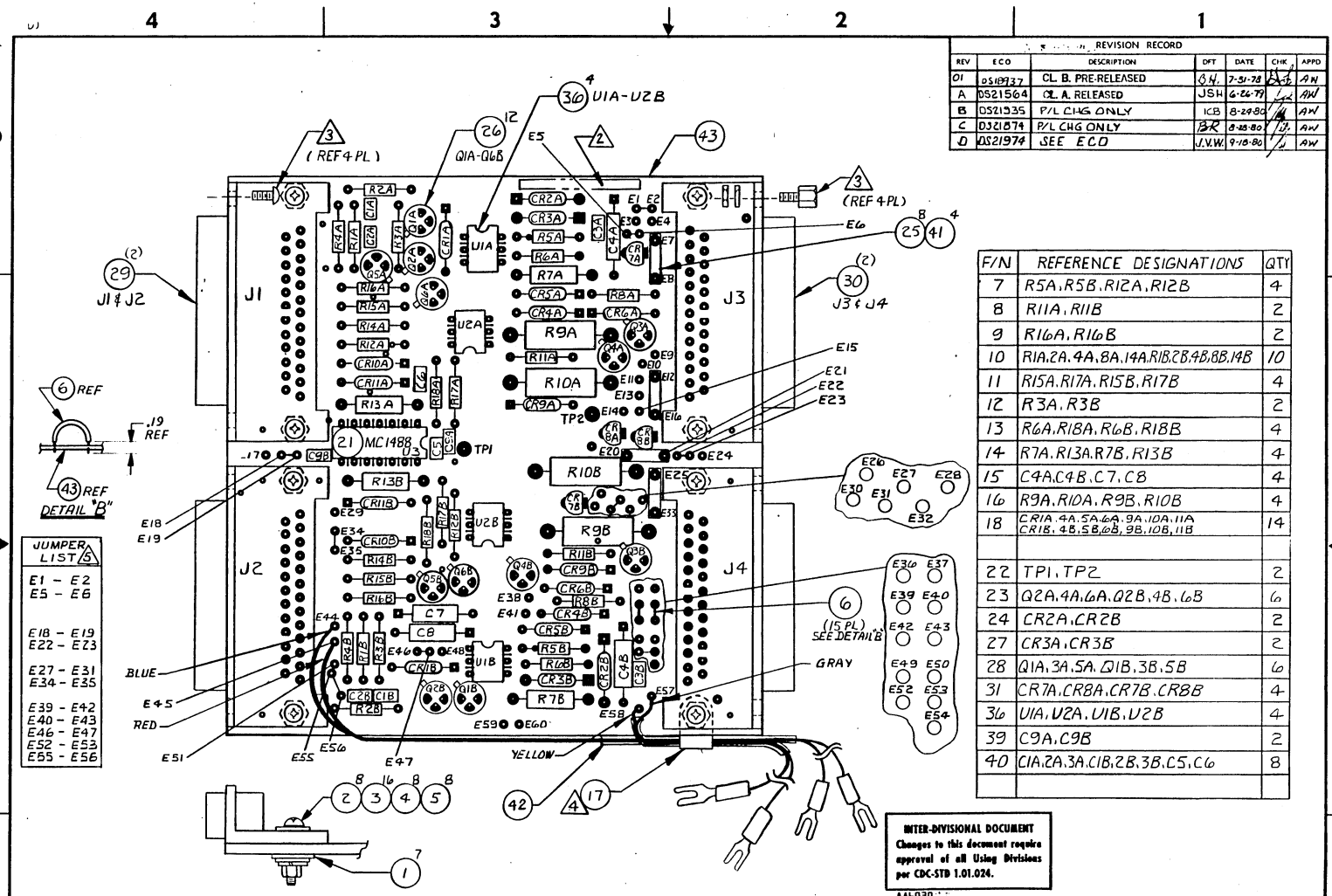

Figure 7-11. Current Loop Adapter Printed Wiring Assembly (Sheet 1 of 3)

DWN	[illegible]	6-6-78	CONTROL DATA CORPORATION	TITLE PWA-BCLA CURRENT LOOP ADAPTER (20MA) 8HRT	PREFIX PL	DOCUMENT NO. 96870310	REV. D
CHKD	[illegible]	7-14-78	DATA SYSTEMS LAJOLLA DIVISION	FIRST USED ON 1843-101 (CYBER 18)		SHEET 1 OF 3	
ENG	M. [illegible]	7-17-78	CODE IDENT 09132				
MFG	[illegible]	6-26-78					
APPR	[illegible]	7-21-78					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	DS018937	CL. B. PRE-RELEASED	C.4	[illegible]	[illegible]	[illegible]
A	DS21564	CL. A. RELEASED	JSH	6-26-79	[illegible]	AW
B	DS21935	F/N 17 WAS 24565001	YB	8-24-80	[illegible]	AW
C	DS21874	F/N 39 WAS 89636104 F/N 40 WAS 89636158	BR	3-28-80	[illegible]	AW
D	DS21974	F/N6 QTY WAS 15	J.Y.W.	9-18-80	[illegible]	AW

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AA6030

NOTES:

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AA3180 REV. 8-71

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CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SH 2

ASSEMBLY NUMBER	REV	CL	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96870310	D	A	C	PWA-BCLA CUR LOOP ADPTR 8HRT	DSM	1843	07/23/78	021974	09/16/80	1/2 MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
17	C	00863701	1 00	PC	CLAMP, CABLE ELECTRICAL	IN	021935	111480			N
1	C	09027801	7 00	PC	WASHER,NONMETALLIC	IN			PPP1		N
2	A	10125103	8 00	PC	HEXAGON MACHINE SCREW NUTS	IN			PPP1		N
3	A	10125603	16 00	PC	PLAIN WASHERS	IN			PPP1		N
4	A	10125801	8 00	PC	SPRING LOCK WASHERS (MED.)	IN			PPP1		N
5	A	10127105	8 00	PC	SCR MACH PAN PHL 4-40	IN			PPP1		N
7	A	17705922	4 00	PC	RES FXD .25 W .27 MEG OHM 5 PC	IN			PPP4		N
8	C	24500033	2 00	PC	RES FXD .25W 56 OHMS	IN			PPP4		N
9	C	24500056	2 00	PC	RES FXD .25W 510 OHMS	IN			PPP4		N
10	C	24500063	10 00	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
11	C	24500070	4 00	PC	RES FXD .25W 2000 OHMS	IN			PPP4		N
12	C	24500074	2 00	PC	RES FXD .25W 3000 OHMS	IN			PPP4		N
13	C	24500077	4 00	PC	RES FXD .25W 3900 OHMS	IN			PPP4		N
14	A	24500150	4 00	PC	RES- FXD CMPSN, 1/2W 300OHMS	IN			PPP4		N
15	C	24504329	4 00	PC	CAP FIXED SOLID TANTALUN	IN			PPP4		N
16	A	24507163	4 00	PC	RES FXD COMP 1W,1000 OHMS	IN			PPP4		N
~~17~~	~~C~~	~~24565001~~	~~1 00~~	~~PC~~	~~CLAMP, CABLE, BLACK NYLON~~	~~OUT~~	021935	111480	PPP4		N
18	A	25175800	14 00	PC	DIODE(1N914)	IN			PPP4		N
21	A	36186400	1 00	PC	IC CHIP,TYPE 1488	IN			PPP4		N
22	A	38838005	2 00	PC	TERM,TUR-SUBMIN,TIN DIP .062	IN			PPP4		N
23	A	38970600	6 00	PC	TRANSISTOR(2N3251)	IN			PPP4		N
24	A	38976300	2 00	PC	DIODE RECT SIM MOTOROLA 1N4001	IN			PPP4		N
25	A	39397400	8 00	PC	SOCKET, MINIATURE SPRING	IN			PPP4		N
26	A	39737600	12 00	PC	MTG PAD TRANSISTOR .250X.021	IN			PPP4		N
27	C	50240914	2 00	PC	DIODE-ZENER,SIL 1 WATT 5 PCT	IN			PPP4		N
28	A	51003092	6 00	PC	XSTR-2N2222,SIL,NPN,HIGH SPEED	IN			PPP4		N
29	A	51873410	2 00	PC	CONN PC RIGHT ANGLE 25 PIN SOC	IN			PPP4		N
30	A	51873411	2 00	PC	CONN,PC RIGHT ANGLE 25 PIN	IN			PPP4		N
31	A	51903806	4 00	PC	DIO LED SLD ST RED DIFF EPOXY	IN			PPP4		N
36	C	72313600	4 00	PC	PHOTOTRANSISTOR OPTO-ISOLAOR	IN			PPP4		N
39	A	75887689	2 00	PC	CAP-CER 330PF, 50DCWV	IN	021874	123081			N
40	A	77830574	8 00	PC	CAP-CERAMIC,0.1UF,50V	IN	021874	123081			N
6	A	88945401	19 00	PC	JUMPER 24AWG TEF INSULATED .60	IN	021974	091680	PPP4		N
~~39~~	~~A~~	~~89636104~~	~~2 00~~	~~PC~~	~~CAP FXD CER 330PF 100VDCW~~	OUT	021874	123081	PPP4		N
~~40~~	~~A~~	~~89636158~~	~~8 00~~	~~PC~~	~~CAP FXD CER .1MFD 100VDCW~~	~~OUT~~	~~021874~~	~~123081~~	~~PPP4~~		N
41	A	89684100	4 00	PC	CONNECTOR PLUG TWO PIN JUMPER	IN			PPP4		N

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Figure 7-11. Current Loop Adapter Printed Wiring Assembly (Sheet 2 of 3)

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

ASSEMBLY NUMBER	REV	CL	OW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CHANGE ORD. NUMBER	PROCESSING DATE	PAGE NUMBER
96870310	D	A	C	PWA-BCLA CUR LOOP ADPTR 8HRT	DSM	1843	07/23/78	021974	09/16/80	2/2 MF

FIND NUMBER	OW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S CM N
42	A	96755035	1.00	PC	HARNESS-CUR LOOP ADAPT DC PWR	IN			AYM4		N
43	C	96870110	1.00	PC	PWB-BCLA CUR LOOP ADPTR	IN			PPP4		N
44	C	96870510	REF	PC	LOGIC-BCLA CUR LOOP ADPTR 8HRT	IN			RFE4		N

NUMBER OF LINE ITEMS = 39
HIGHEST FIND NUMBER = 44

SCMD-1 REV 2-80 MFG INFO

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Figure 7-11. Current Loop Adapter Printed Wiring Assembly (Sheet 3 of 3)

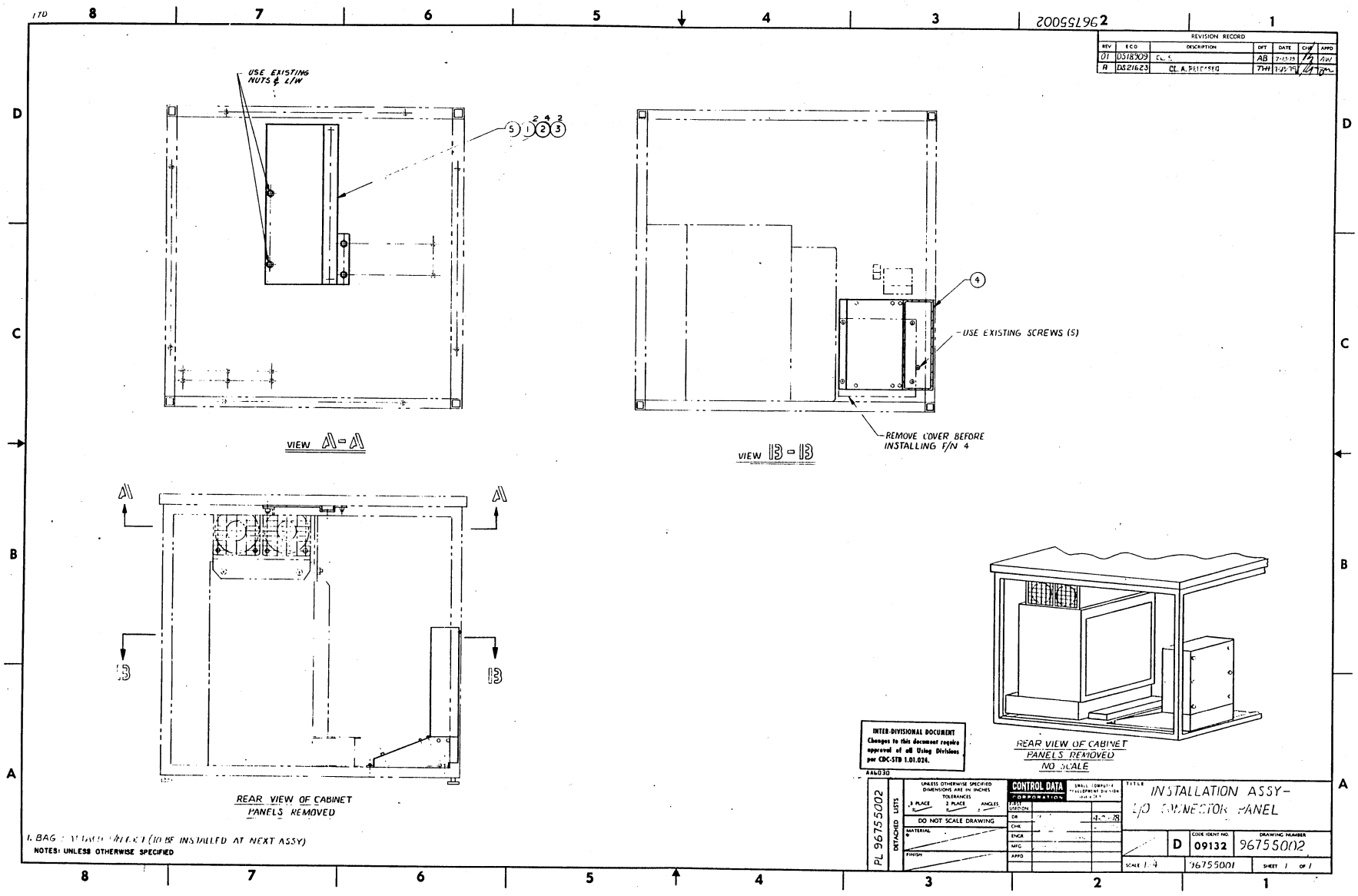

Figure 7-12. I/O Connector Panel Installation Assembly (Sheet 1 of 2)

ITD

DWN	[illegible]	4-26-78	CONTROL DATA CORPORATION	TITLE: INSTL ASSY- I/O CONN PANEL	PREFIX: PL	DOCUMENT NO.: 96755002	REV.: A
CHKD	[illegible]	4-27-78					
ENG	[illegible]	7-10-78	DATA SYSTEMS LA JOLLA DIVISION	FIRST USED ON		SHEET 1 OF 2	
MFG	[illegible]	7-10-78	CODE IDENT 09132				
APPR	[illegible]	7-13-78					

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	DS18909	CL. B. PRE-RELEASED	AB	7-13-78	[illegible]	AW
A	DS21623	CL. A. RELEASED	TWH	7-23-79	[illegible]	[illegible]

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AALD80 ITD

NOTES:

DETACHED LISTS

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CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH 2
MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96755002	A	CLA	D	INSTL ASSY-I/O CONN PANEL	USM	C8R 18	07/10/78	07/18/79	

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
1	A	10125106	200	PC	HEXAGON MACHINE SCREW NUTS	IN			PPP1		N
2	A	10125606	400	PC	PLAIN WASHERS	IN			PPP1		N
3	A	10125804	200	PC	SPRING LOCK WASHERS (MED.)	IN			PPP1		N
4	D	88951306	100	PC	CABLE ENTRY ASSY	IN			AYM4		N
5	C	88951308	100	PC	CABLE RETAINER	IN			PPP4		N
6	C	94277419	800	PC	STRAP CABLE TIE	IN			PPP3		N
7	A	96744964	800	PC	SCREW-THD ROLL 6-32 1/4 LG	IN			PPP3		N

NUMBER OF LINE ITEMS = 7
HIGHEST FIND NUMBER = 7

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AA 2709-1 REV. 7-75

Figure 7-12. I/O Connector Panel Installation Assembly (Sheet 2 of 2)

GLOSSARY A

This appendix consists of an alphabetical listing of acronyms and mnemonics used in this manual. For convenience, all mnemonics for signal names are presented in the true or conventional state, although some signal names exist only in the false or reverse level state.

ALU	Arithmetic logical unit
BCLA	Buffered communication line adapter
BFE	Break or framing error
BMV	Block move operation
BRK	Break detect
CPE	Channel parity error
CPU	Central processor unit
CR	Carriage return
CTS	Clear to send
DCD	Data carrier detect
DIP	Dual inline package
DMA	Direct memory access
DSR	Data set ready
DTR	Data terminal ready
EOT	End of text
ESW	Extended status word
EXT	Extended status
FCO	Field change order
FE	Framing error
FG	Frame ground
FWA	First word address
FWA-H	First word address high-order bits
I/O	Input/output
LBT	Loop-back test mode
LDE	Last data error
LF	Line feed
LSB	Least significant bit
M	An interrupt caused by completion of a block move operation
MAB	Memory address bit
MAE	Memory address error
MDM	An interrupt caused by the change of state of modem lines DCD or DSR
MOS	Metal oxide semiconductor
MPR	Memory parity error
MR	Memory read operation
MSB	Most significant bit
MW	Memory write operation
NIP	No interrupt pending
OE	Overrun error
P	Port or channel
PE	Parity error
PWA	Printed wiring assembly
R	Receive/receiver
RCV	Receive/receiver
RD	Receive data
ROM	Read-only memory
RTS	Request to send
SG	Signal ground
SR	Data signal rate select
T	Transmit/transmitter
TD	Transmit data
TMT	Transmit/transmitter
TTL	Transistor-to-transistor logic
U	Unused/undefined
USART	Universal synchronous/asynchronous receiver/transmitter
USRT	Universal synchronous receiver/transmitter

FIRMWARE INSTRUCTIONS B

This appendix contains a firmware instruction list and a description of the firmware fields. The firmware instruction list includes the micro-instruction field equates, instruction codes, code equivalences, code symbols, and alphabetical sorts of symbols. The description of the firmware fields describes how each of the 10 fields of the micro instruction are employed in each instruction.

FIELD EQUATES

The field equates, pages A4 through A8 of the firmware list, indicate the selections that are available to each field and the hexadecimal code that determines the individual selections.

REGISTER FILE MAP

The file map, page 9, indicates the structure and content of the common controller file register.

INSTRUCTION CONTENTS

The firmware contains the 64-bit micro instructions that control the flow of commands, data, and status words between the BCLA interface, the controller, and the processor. These firmware instructions also control the internal operations of the controller elements. Each instruction word consists of two 32-bit instructions (figure B-1) that comprise 10 fields of selection; the two enable (E) fields are combined as one function. Each line in the listing contains the assembler line number, assembler memory address, ROM memory address of each 64-bit word, hexadecimal value of each 32-bit instruction, firmware field selections, and a brief statement of operational action.

ASSEMBLER PROGRAM STATEMENT, LINE NUMBER

This number is a sequential numbering of the input deck cards.

ASSEMBLER PROGRAM, MEMORY ADDRESS

This hexadecimal number list indicates the 1700 memory address of the assembled program in which the micro instruction address and associated field data reside.

ROM ADDRESS

This number indicates the address in the read-only memory (ROM) chip where the micro instruction (64-bits) resides.

MICRO INSTRUCTION

These four numbers (figure B-2) are hexadecimal notations of the upper and lower 32-bit instructions contained in the 64-bit micro instruction. These hexadecimal notations are arranged in four 16-bit groups of which each digit represents four bits of the upper or lower half of the 32-bit micro instruction.

SEQUENCE FIELD

The SEQ field (bits 30 and 31) controls the loading and incrementing of the instruction address counter. Refer to table B-1 for sequence bit operations.

TABLE B-1. SEQUENCE FIELD

Bits		Mnemonic	Operation
30	31		
0	0	XFM	Transform, load instruction address from ALU
0	1	JPT	Jump, load instruction address from F2/F3
1	0	CMA	Current micro address, do not change instruction address
1	1	SEQ	Sequential, increment instruction address

A plus sign (+) immediately following the sequence code mnemonic indicates to the assembler that this is an upper instruction. This plus sign causes the instruction address to be inserted to designate the address of the next four hexadecimal notations; the first two words (32 bits) are the upper instruction and the last two words are the lower instruction.

CONDITION FIELD

The COND field (bits 27 through 29) feeds the selected auxiliary condition inputs to the main condition multiplexer. The selected condition determines whether the next instruction is the upper or lower 32 bits of the instruction word.

ASSEMBLER PROGRAM STATEMENT LINE NUMBER

ASSEMBLER PROGRAM MEMORY ADDRESS

0000, 0001, 0002: ROM ADDRESS OF EACH 64-BIT MICRO INSTRUCTION

C7E6: UPPER 32-BIT MICRO INSTRUCTION
FDC0: LOWER 32-BIT MICRO INSTRUCTION

MICRO-INSTRUCTION IDENTIFIER; TAG

```
0280                    S

0280   P0000   0000
0280   P0001   87AB
0289   P0002   2CEF
0281
0281   P0003   C7E6
0281   P0004   FDC0
0282
0282   P0005   0001
0282   P0006   EFFE
0282   P0007   34AF
0283                    ZIF
0283   P0008   9FE7
0283   P0009   E5FF
0284
0284   P0010   0002
0284   P0011   D7FE
0284   P0012   1AEF
0285
0285   P0013   4386
0285   P0014   EF01
```

SEQUENCE	CONDITION	S1	ALU	S2	DESTINATION	ENABLE	F1	F2	F3	OPERATION STATEMENT
CMA+	LOWER	NU	S2	CST	PORTDL	E1	STBC1	SETBRG	NU	RST PRT (9600 B)
SEQ	LOWER	NU	ZERO	NU	FA	EB	CLRUDC	LDPCR	$0	SEG=0, LBT OFF BIT
SEQ+	FRAEQF	NU	NU	NU	NONE	EB	INCFPA	SETTM	NU	FRA=F TO GET HERE
CMA	FRAEQF	NU	ZERO	NU	L2F	E1	INCTFA	NU	NU	WRITE ZERO TO FRA
SEQ+	AUX1	NU	NU	NU	NONE	E2	SEGEQ3	CNTUP	NU	FPA=F TO GET HERE
JPT	LOWER	FAD	S1	NU	FA	E1	LDPNR	ZTF		FPA NOT F

Figure B-1. Firmware Program List Instruction Format

```
0280                    S       CMA+ LOWER, NU, S2, CST, PORTDL, E1, STBC1, STBRG, NU
0280    P0000   0000
0280    P0001   87AB
0280    P0002   2CEF
0281                            SEQ LOWER, NU, ZERO, NU, FA, EB, CLRUDC, LDPCR, $0
0281    P0003   C7E6
0281    P0004   FDC0
```

UPPER FOUR DIGITS				LOWER FOUR DIGITS			
8 C	7 7	A E	B 6	2 F	C D	E C	F 0

31 30	29 28 27	26 25 24 23	22 21 20 19	18 17	16 15 14	13	12	11 10 9 8	7 6 5 4	3 2 1 0
SEQ.	COND.	S1	ALU	S2	DEST.	E1	E2	F1	F2	F3

Figure B-2. Upper and Lower 32-Bit Micro-Instruction Hexadecimal Format Derivation

S1 Field

This field (bits 23 through 26) selects the inputs from the common controller communication interface to the A inputs of the ALU via the S1 bus. Values 0 through 7 are applicable to the common controller and values 8 through F are applicable to the communication interface.

ALU Field

This field (bits 19 through 22) feeds the four main control inputs (S0 through S3) of the ALU. These inputs select one of 16 logical operations. The arithmetic operations are selected by the F1 field enable signal being applied to the ALU M input. This M input enables the carries within the ALU to select the arithmetic operation with carry in (ARITHC) and without carry in (ARITHN).

S2 Field

The S2 field (bits 17 and 18) selects the common controller inputs to the B inputs of the ALU via the S2 bus.

DESTINATION FIELD

The DEST field (bits 14 through 16) determines the register that shall receive the ALU output at the end of the instruction. File writes (data storage) are also specified by this field.

E1 and E2 Fields

These two fields (bits 13 and 12, respectively) are combined and designated as on field in the instruction word listing. The E1 bit enables or activates the selections of the F1 field and the E2 enables selections of the F2 field.

F1 Field

This field (bits 08 through 11) selects the F1 strobes and enables, the bit generator output bit, the auxiliary conditions of the communication interface, and the auxiliary conditions of the common controller.

F2 Field

This field (bits 04 through 07) selects the F2 enables, F2 strobes, and control bits selector of the common controller. This field is also combined with the F3 field for updating the instruction addresses for jump operands, provides constants to the ALU as required by the firmware, and provides a direct file address.

F3 Field

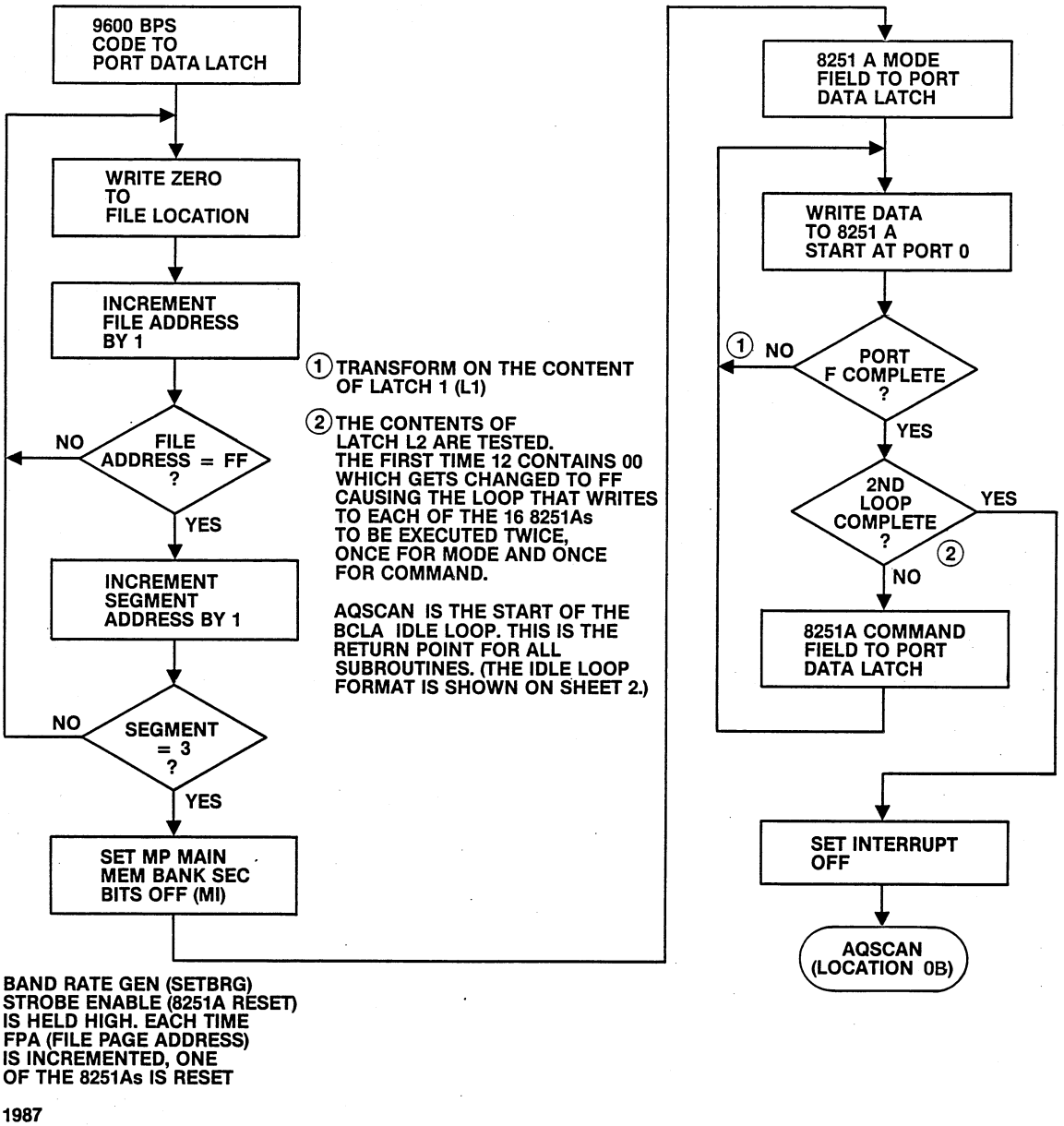
This field (bits 00 through 03) combines with the F2 field for some operations. Refer to the F2 field description.

FLOWCHARTS

Figure B-3 is a flowchart illustration of the BCLA firmware program contained in appendix C. Appendix C can be used to determine the actual read-only memory cell location of a particular flowblock.

MASTER RESET

THIS ROUTINE STARTS AT ROM ADDRESS 00 AND IS ENTERED BY PRESSING THE CONSOLE MASTER CLEAR OR BY A JUMP FROM LOCATION 27 WHEN A SOFTWARE MASTER CLEAR FUNCTION IS ISSUED.



(1) TRANSFORM ON THE CONTENT OF LATCH 1 (L1)

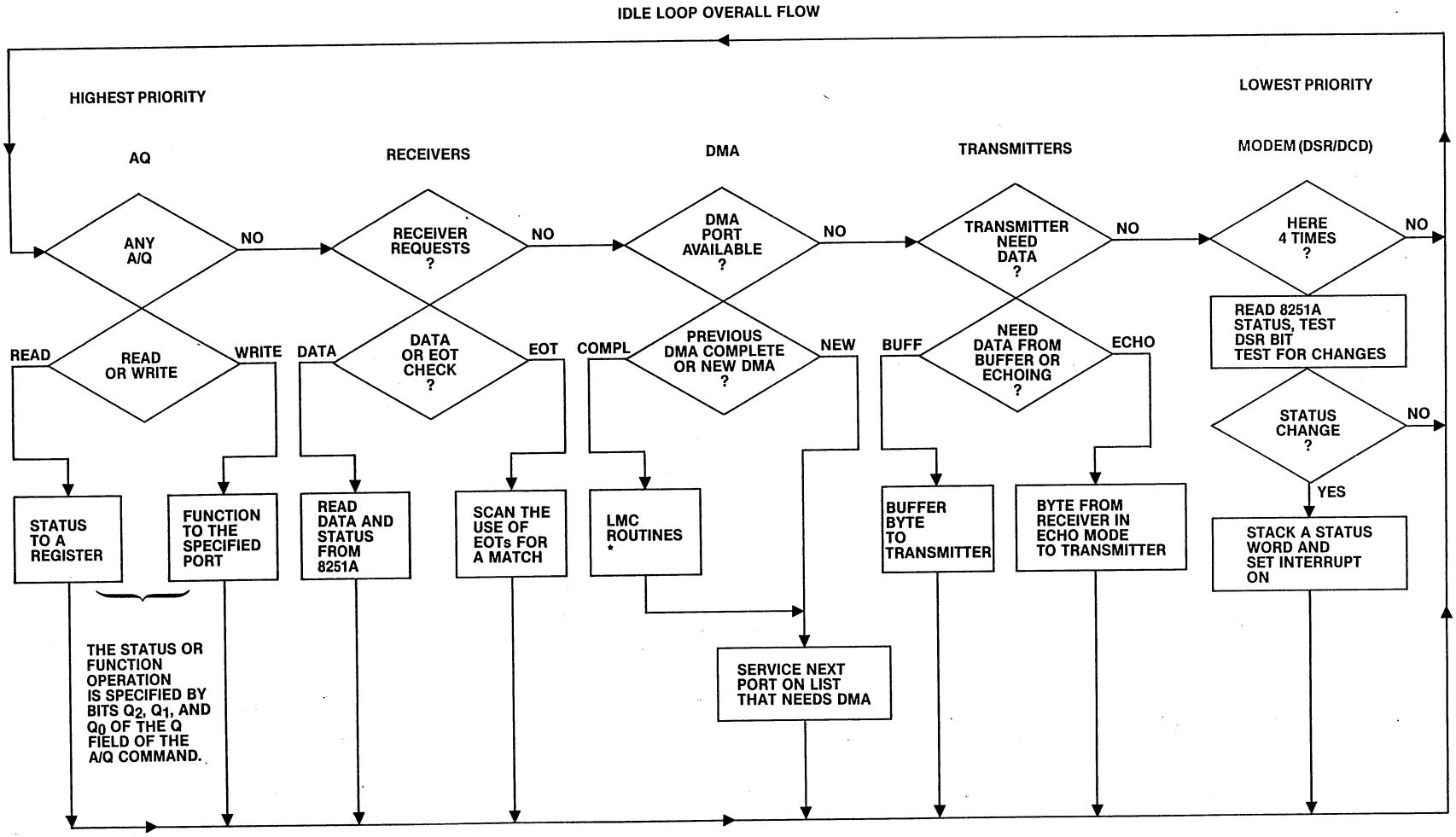
(2) THE CONTENTS OF LATCH L2 ARE TESTED. THE FIRST TIME 12 CONTAINS 00 WHICH GETS CHANGED TO FF CAUSING THE LOOP THAT WRITES TO EACH OF THE 16 8251As TO BE EXECUTED TWICE, ONCE FOR MODE AND ONCE FOR COMMAND.

AQSCAN IS THE START OF THE BCLA IDLE LOOP. THIS IS THE RETURN POINT FOR ALL SUBROUTINES. (THE IDLE LOOP FORMAT IS SHOWN ON SHEET 2.)

BAND RATE GEN (SETBRG) STROBE ENABLE (8251A RESET) IS HELD HIGH. EACH TIME FPA (FILE PAGE ADDRESS) IS INCREMENTED, ONE OF THE 8251As IS RESET

1987

Figure B-3. BCLA Firmware Listing Flowchart (Sheet 1 of 16)



*LMC (LAST MEMORY CYCLE WAS):
- LMCTF — TRANSMITTER FETCH (BUFFER DATA FOR A TRANSMITTER)
- LMCRS — RECEIVER STORE (RECEIVER DATA TO A BUFFER)
- LMCMF — BLOCK MOVE FETCH (BUFFER DATA FROM SOURCE)
- LMCMS — BLOCK MOVE STORE (DATA TO DESTINATION BUFFER)

Figure B-3. BCLA Firmware Listing Flowchart (Sheet 2 of 16)

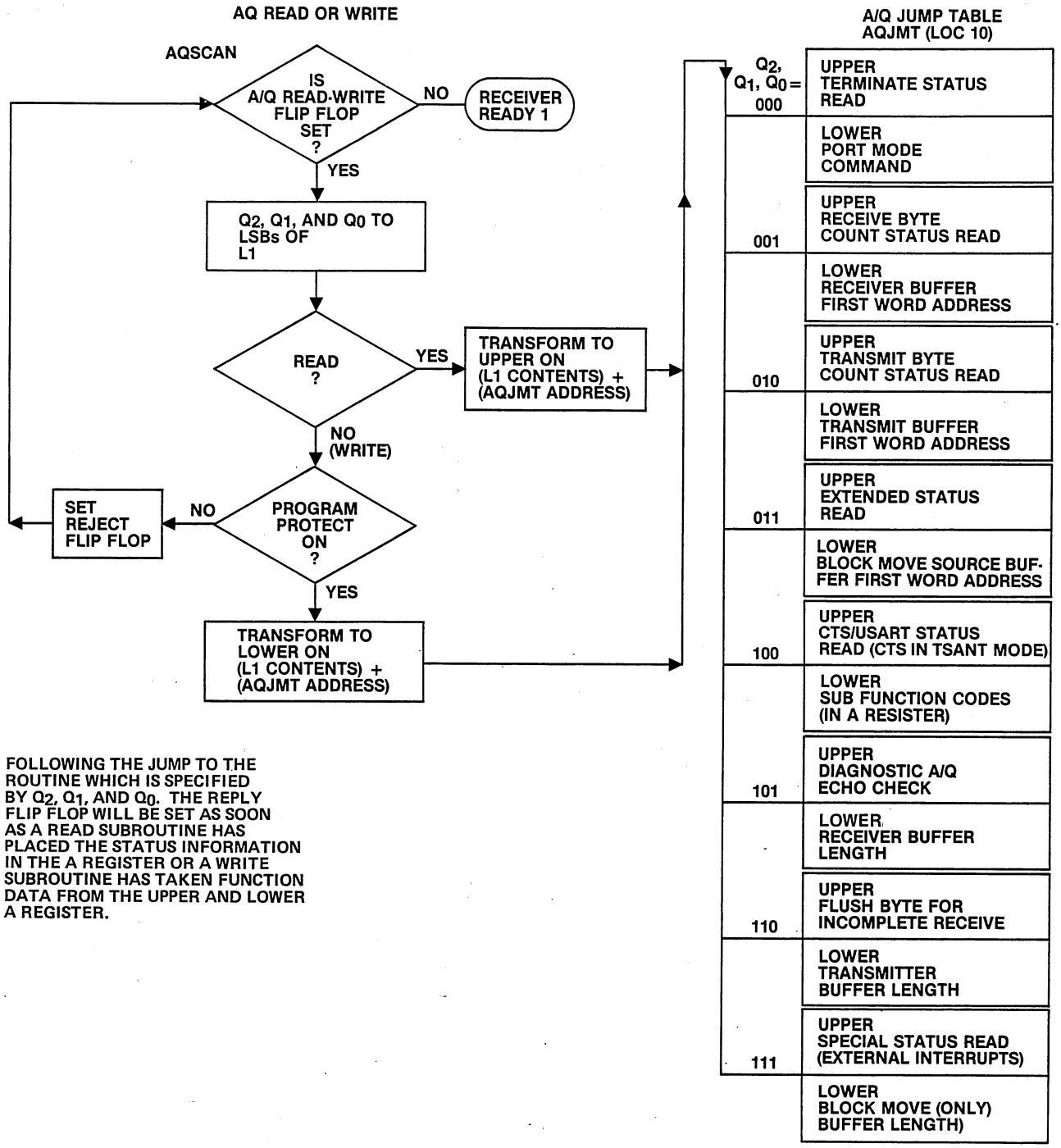


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 3 of 16)

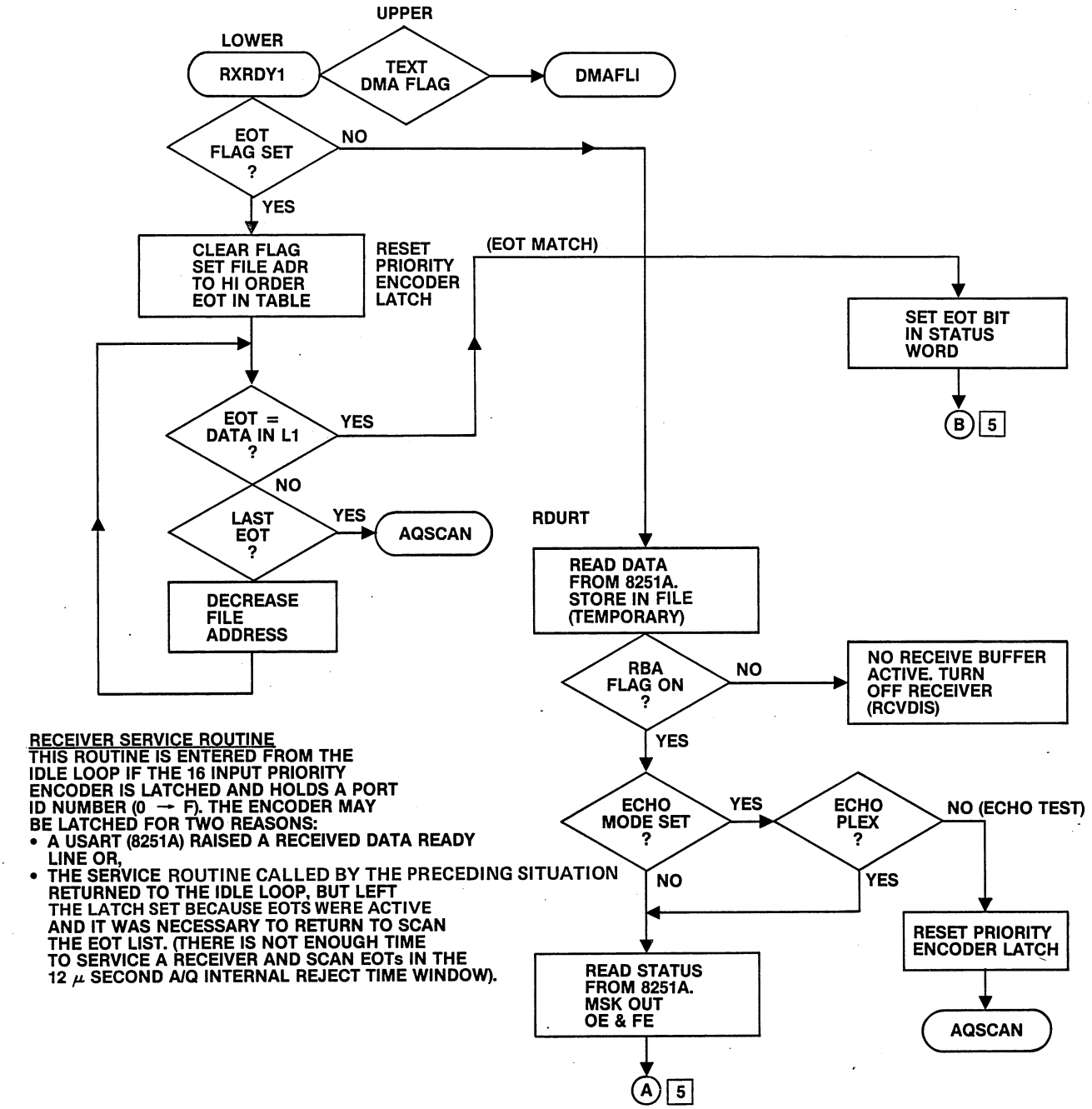


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 4 of 16)

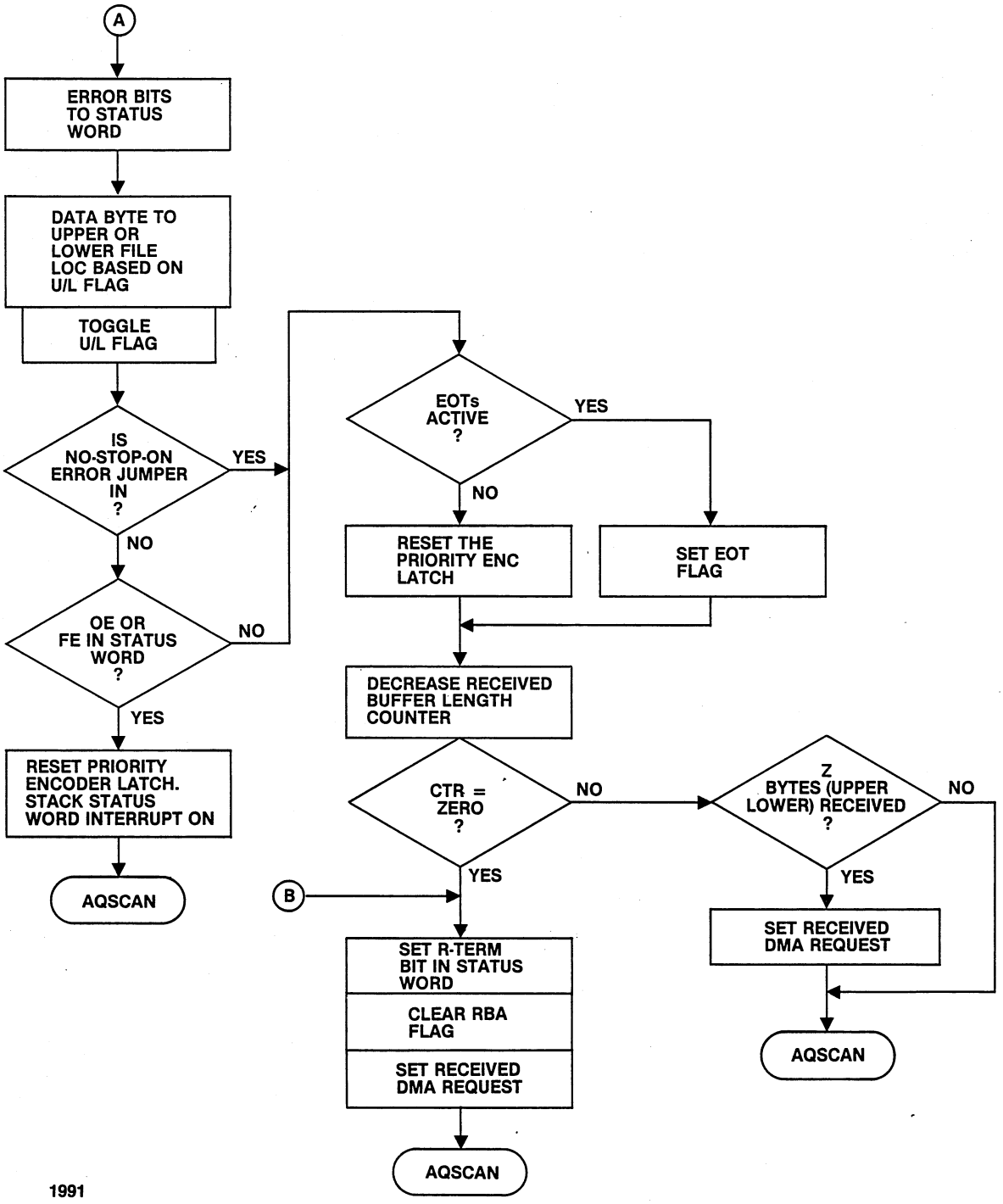


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 5 of 16)

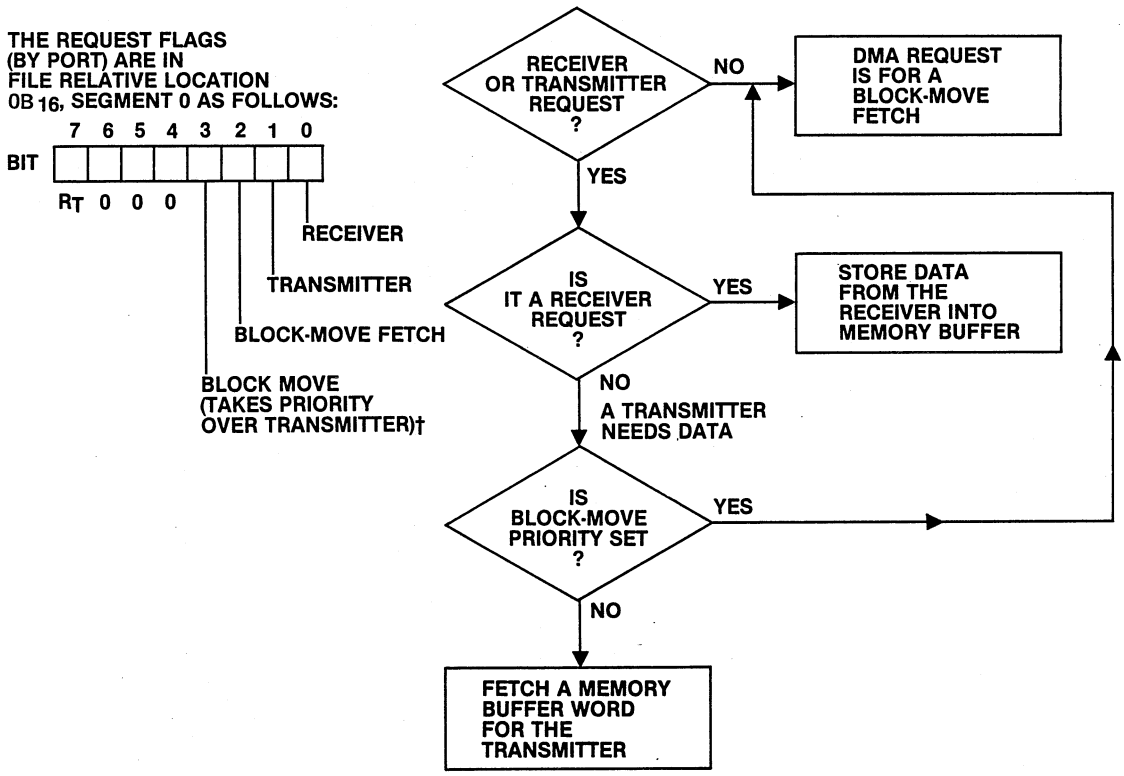
DMA ROUTINES
THESE ROUTINES ARE ENTERED IF THE DMA PORT IS AVAILABLE (NOT BUSY). IF IT IS NOT BUSY, THERE ARE TWO POSSIBLE ACTIONS:
(1) A DMA HAS JUST COMPLETED AND THE DATA JUST TRANSFERRED INDICATES FURTHER ACTION, OR

(2) THE DMA PORT HAS BEEN IDLE AND MAY BE USED FOR ANY PENDING DMA REQUESTS. (AT EACH PASS THROUGH THE IDLE LOOP, ONLY ONE PORT IS CHECKED FOR SERVICE REQUESTS.)

ANY PORT MAY BE REQUESTING DATA FOR ITS TRANSMITTER, A STORE TO A BUFFER FOR RECEIVED DATA, OR A FETCH OF DATA FOR A BLOCK MOVE. ALL REQUESTS COULD BE UP SIMULTANEOUSLY. IF THEY ARE, THE FOLLOWING PRIORITY SCHEME IS USED TO SERVICE THEM. NOTE THAT ONLY ONE TYPE WILL BE SERVICED AND THE IDLE LOOP WILL GIVE THE OTHER 15 PORTS A CHANCE TO USE DMA BEFORE THE LOWER PRIORITY REQUEST FOR A PORT WILL BE SERVICED.

DMA ROUTINGS START ON SHEET 7.

INDIVIDUAL PORT DMA REQUEST SERVICE PRIORITY SCHEME



†THIS CONDITION IS USED WHEN A BLOCK-MOVE WITH TRANSMIT OPERATION IS REQUESTED THE BLOCK MOVE WILL TAKE PRIORITY FOR THE FIRST 2 WORD FETCHES TO ASSUME THAT THE TRANSMITTER HAS DATA IN ITS BUFFER (ALWAYS THE SAME AS THE BLOCK-MOVE DESTINATION BUFFER)

1992

Figure B-3. BCLA Firmware Listing Flowchart (Sheet 6 of 16)

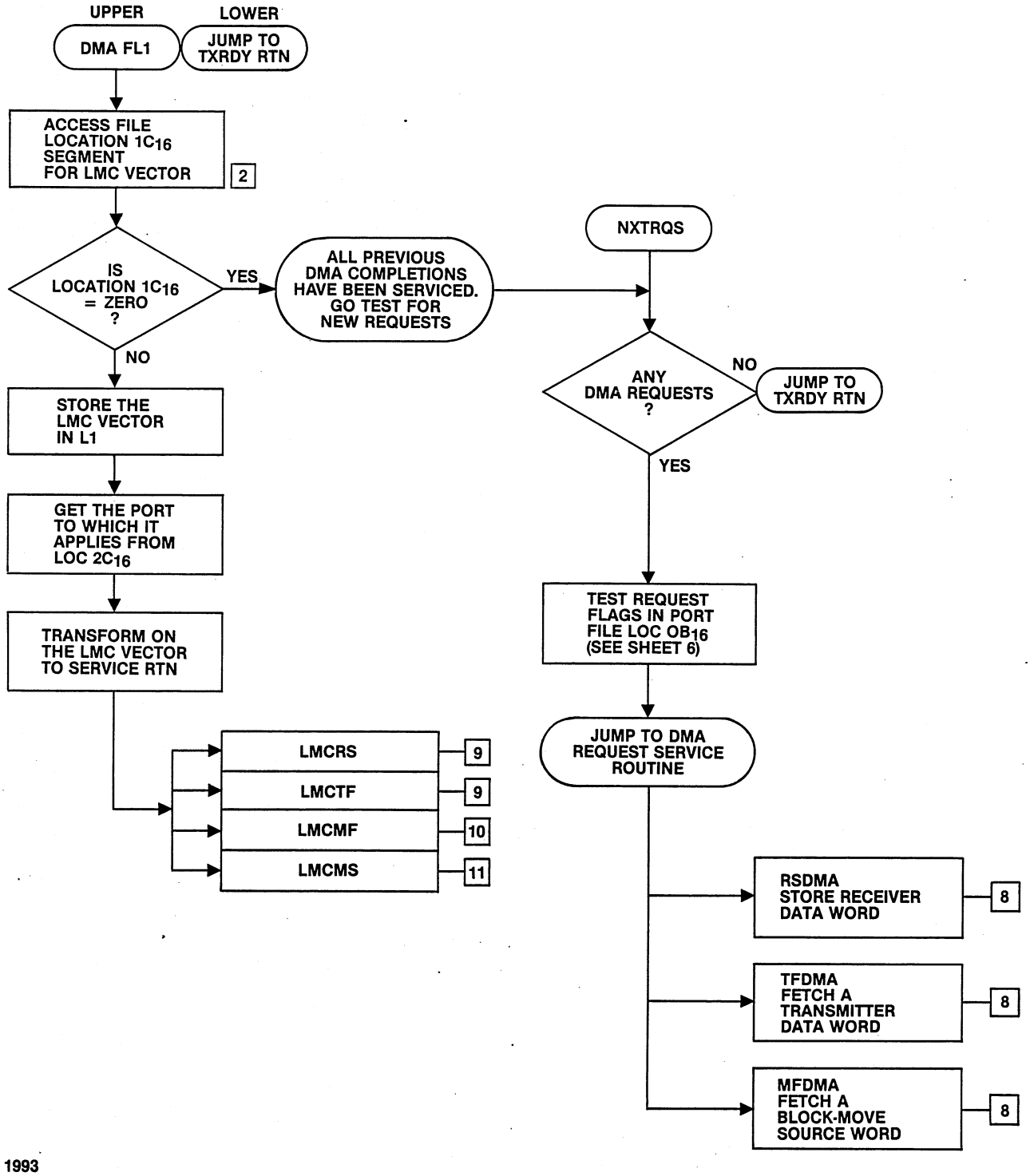


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 7 of 16)

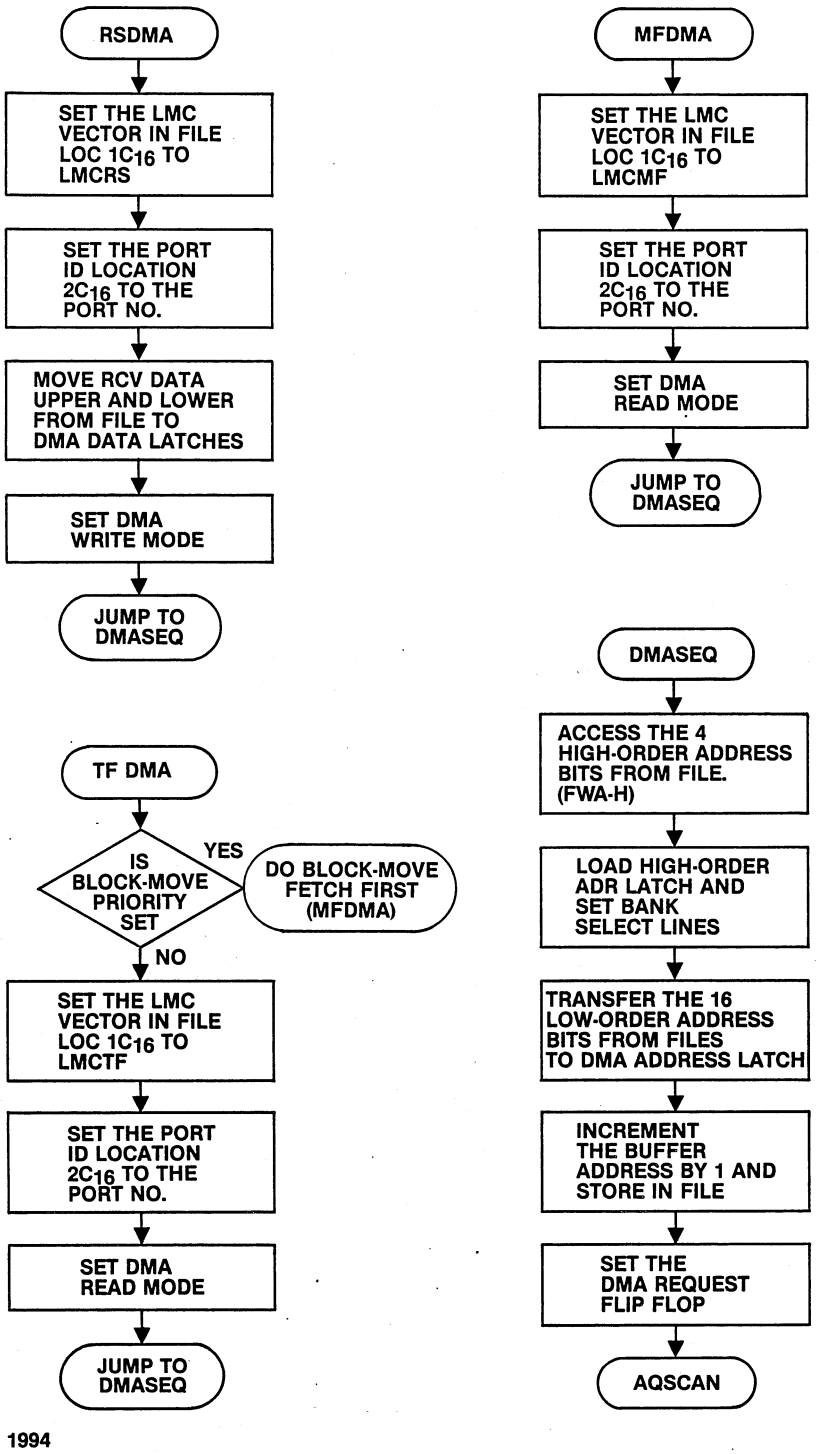


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 8 of 16)

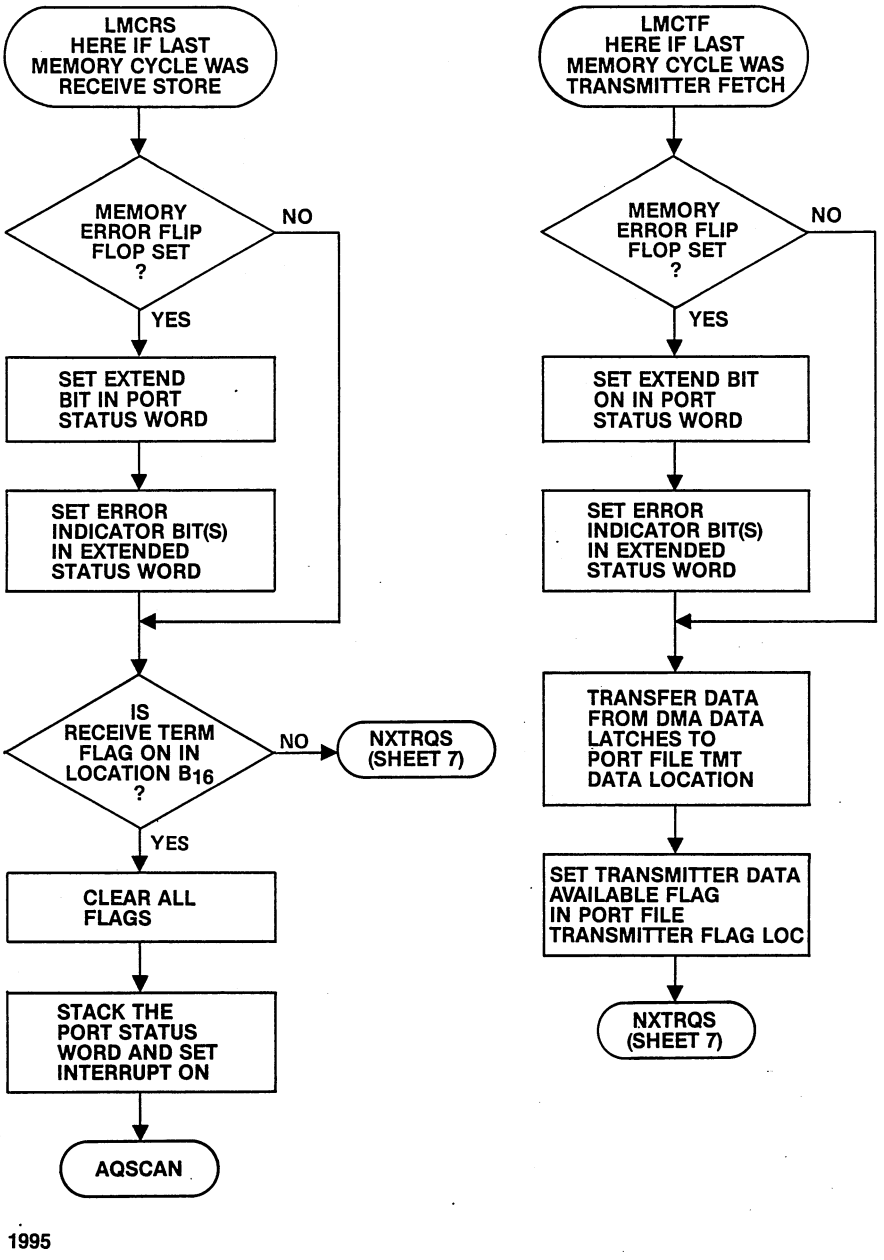


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 9 of 16)

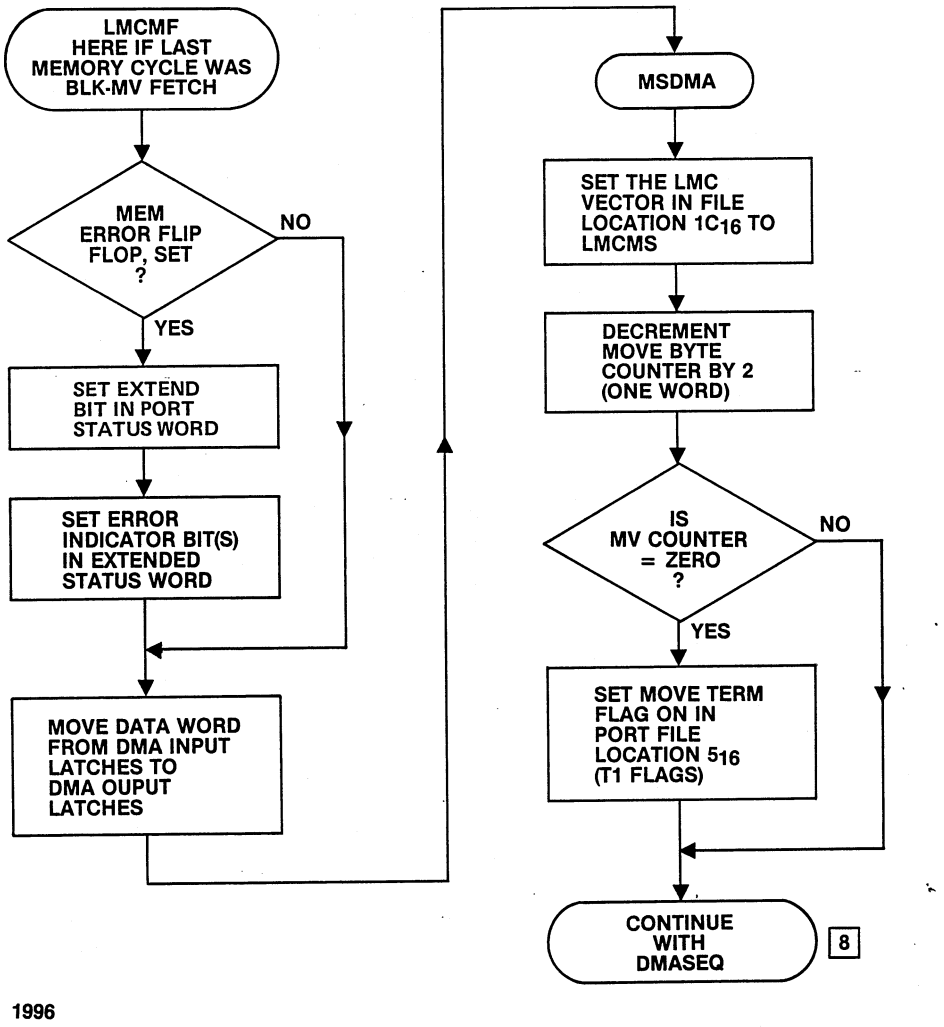
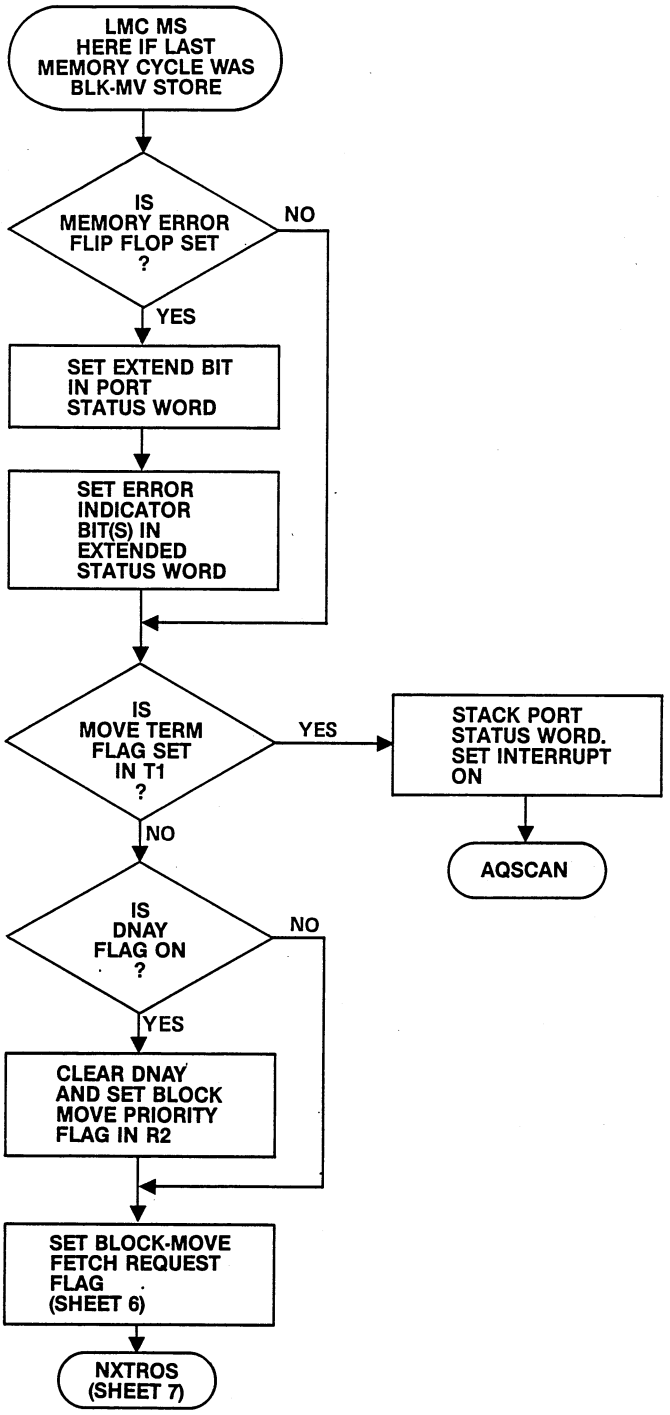


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 10 of 16)



DNAY — DATA NOT AVAILABLE YET (TO TRANSMITTER)

IF FLAG IS SET, IT IS THE FIRST WORD OF THE BLOCK MOVE THAT HAS JUST BEEN STORED; THEREFORE, CLEAR THE FLAG HERE AND REQUEST PRIORITY BLOCK MOVE ONE MORE TIME. AFTER THAT, THE TRANSMITTER WILL ASSUME PRIORITY OVER BLOCK MOVE.

1997

Figure B-3. BCLA Firmware Listing Flowchart (Sheet 11 of 16)

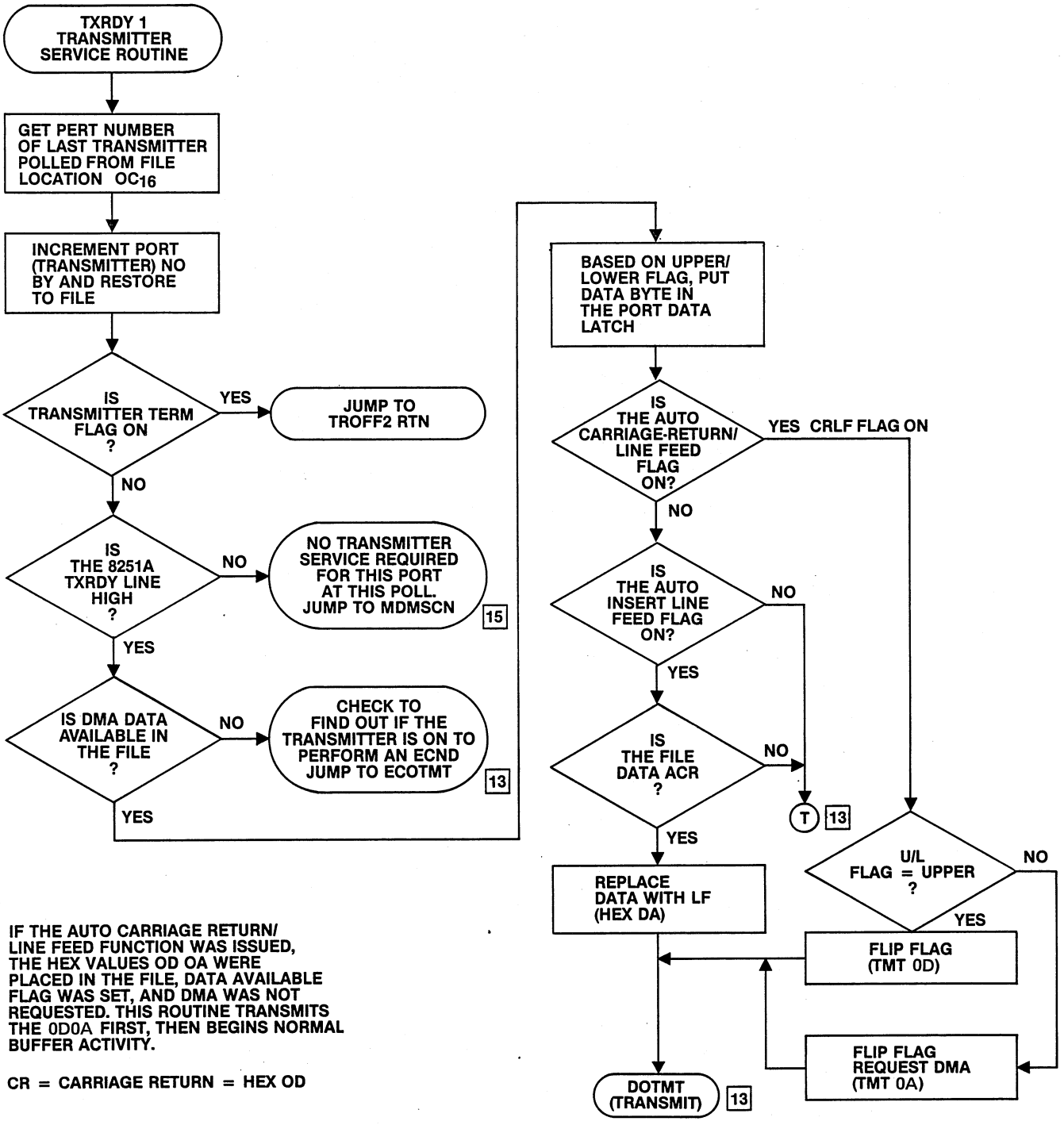


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 12 of 16)

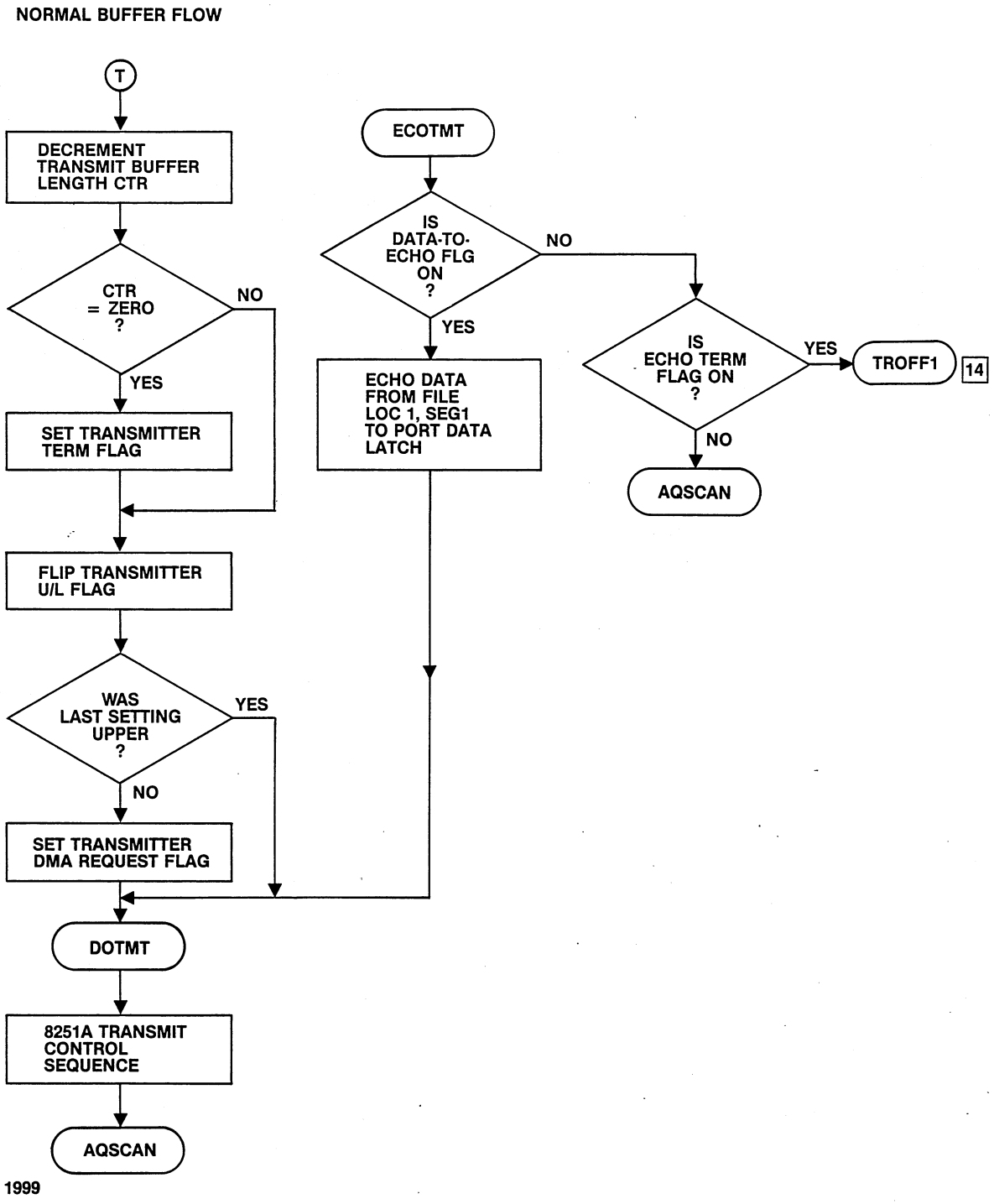


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 13 of 16)

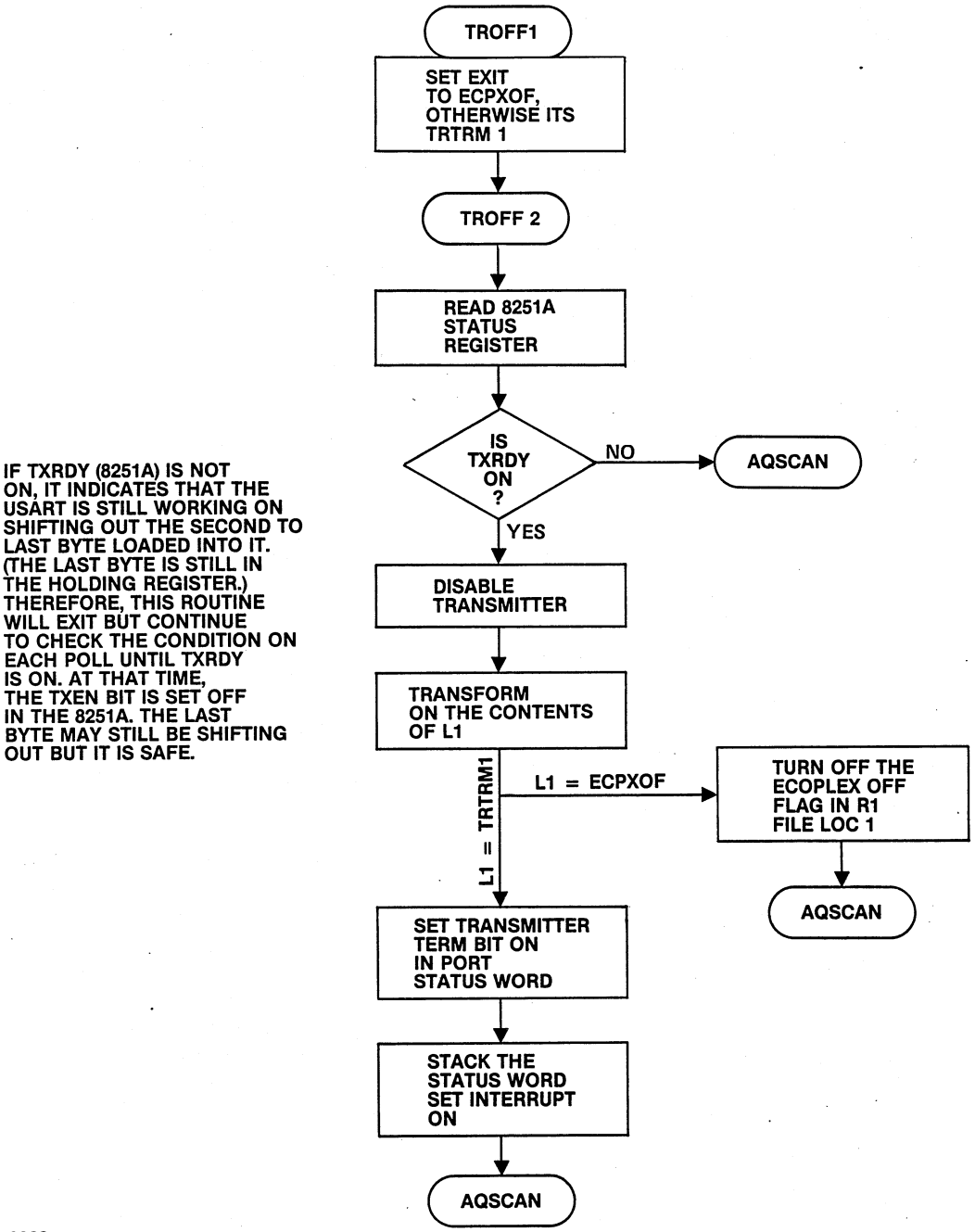


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 14 of 16)

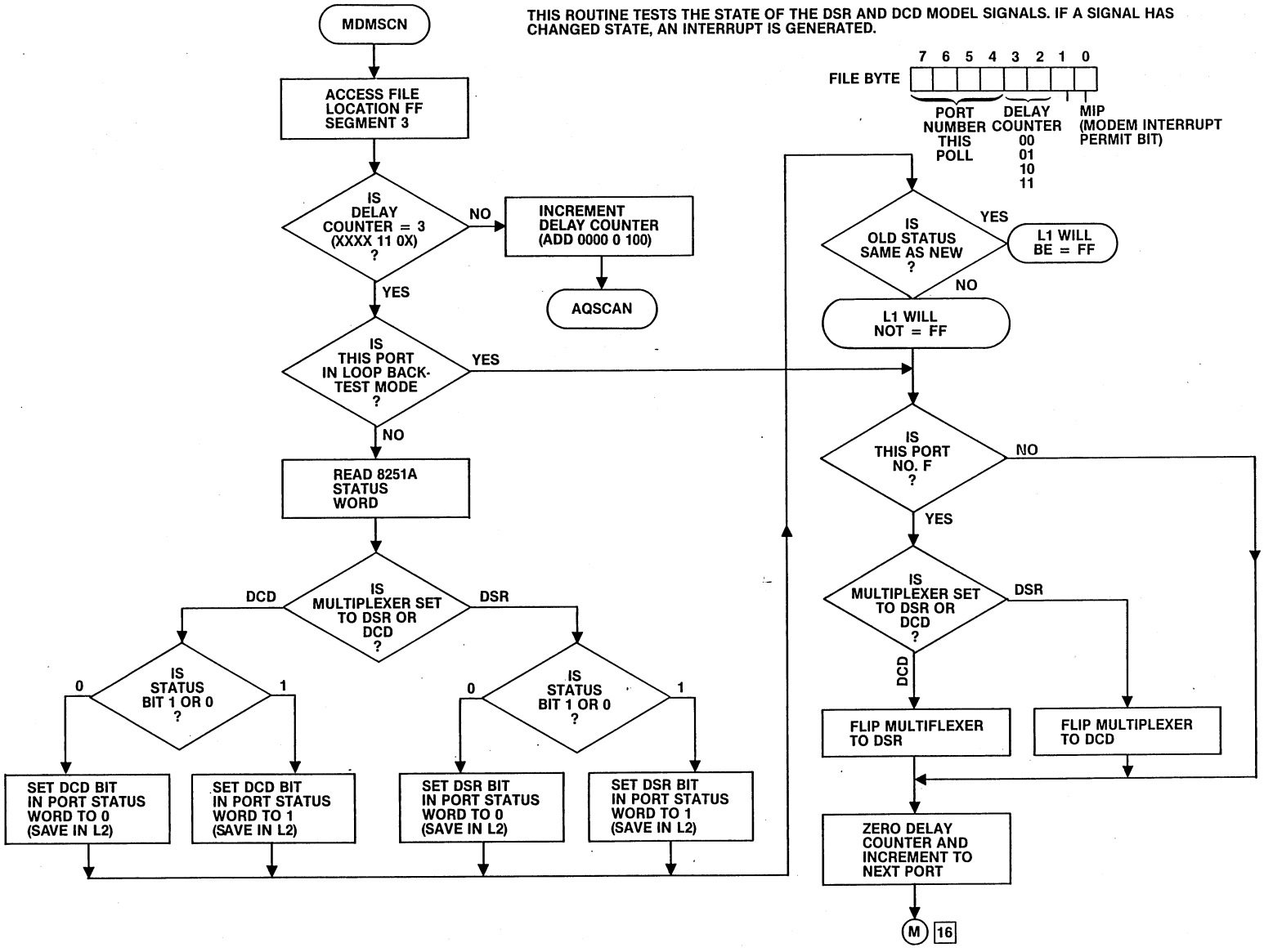


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 15 of 16)

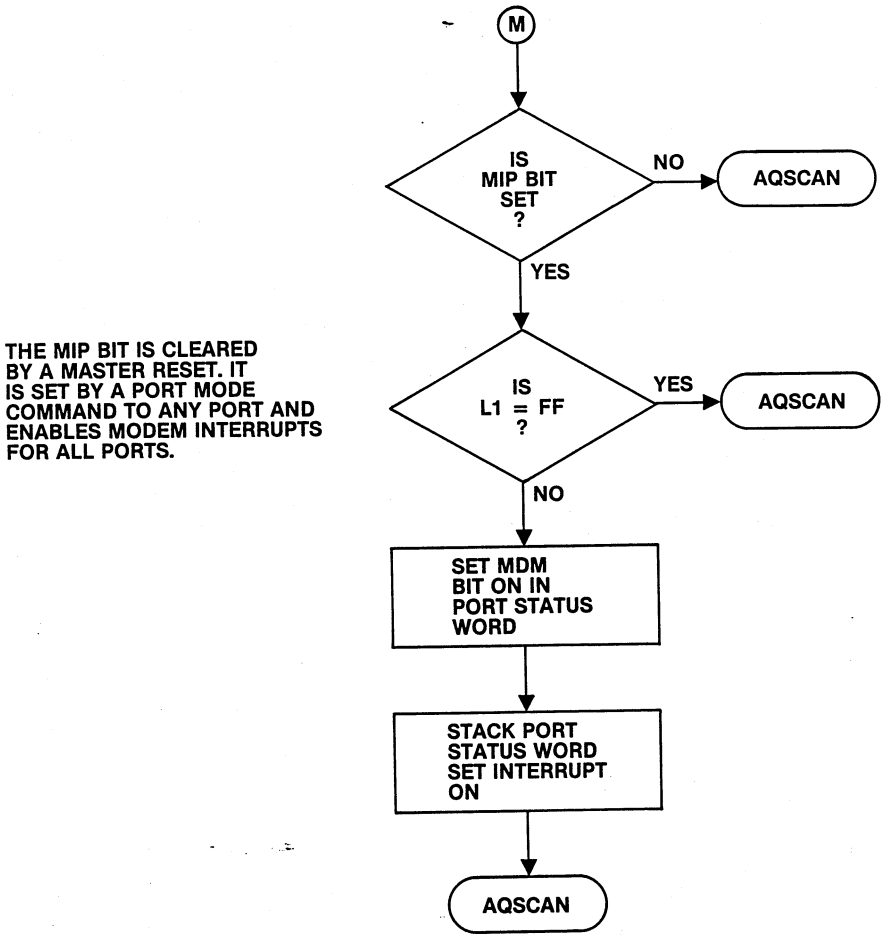


Figure B-3. BCLA Firmware Listing Flowchart (Sheet 16 of 16)

```
BCLAFW              PAGE   1              DATE: 05/23/79


0001                    NAM  BCLAFW
0002              JPT    MAC  CD,SO,AU,ST,DS,EE,F1,F2                    JUMP
0003                     IFC  '.',EQ,+
0004                     IFA  N,EQ,5
0005                     ADC  */N-S/N
0006                     EIF
0007                     VFD  N2/1,X3/'CD',X4//'SO',X4//'AU',X2//'ST',X1//'DS'/4
0008                     VFD  X2//'DS',X2//'EE',X4//'F1',X8//'F2'/N-S/N
0009                     EMC
0010              CMA    MAC  CD,SO,AU,ST,DS,EE,F1,F2,F3              CURRENT MICRO ADD.
0011                     MS'.' 2,'CD','SO','AU','ST','DS','EE','F1','F2','F3'
0012                     EMC
0013              SEQ    MAC  CD,SO,AU,ST,DS,EE,F1,F2,F3              SEQUENTIAL
0014                     MS'.' 3,'CD','SO','AU','ST','DS','EE','F1','F2','F3'
0015                     EMC
0016              XFM    MAC  CD,SO,AU,ST,DS,EE,F1,F2,F3              TRANSFORM
0017                     MS'.' 0,'CD','SO','AU','ST','DS','EE','F1','F2','F3'
0018                     EMC
0019              FIL    MAC  P1                                      FILL
0020                     IFC  '.',EQ,+
0021                     IFA  N,EQ,5
0022                     ADC  */N-S/N
0023                     EIF
0024                     IFC  '.',EQ,+
0025                     NUM  -$77FF,0
0026                     EIF
0027                     IFC  '.',NE,+
0028                     NUM  -$7FFF,0
0029                     EIF
0030                     EMC
0031              MS     MAC  SQ,CD,SO,AU,ST,DS,EE,F1,F2,F3
0032                     IFC  '.',EQ,+
0033                     IFA  N,EQ,5
0034                     ADC  */N-S/N
0035                     EIF
0036                     IFC  ,EQ,'F3'
0037                     VFD  N2/'SQ',X3/'CD',X4//'SO',X4//'AU',X2//'ST',X1//'DS'/4
0038                     VFD  X2//'DS',X2//'EE',X4//'F1',X8//'F2'
0039                     EIF
0040                     IFC  ,NE,'F3'
0041                     VFD  N2/'SQ',X3/'CD',X4//'SO',X4//'AU',X2//'ST',X1//'DS'/4
0042                     VFD  X2//'DS',X2//'EE',X4//'F1',X4//'F2',X4//'F3'
0043                     EIF
0044                     EMC


0046              ********************************************************************
0047              *       ADDRESS WORD EQUATE.                                       *
0048              *       SET N = 5 FOR ADDRESS WORD.                                *
0049              *       SET N = 4 FOR NO ADDRESS WORD.                             *
0050              ********************************************************************

0052        0005          EQU  N(5)
```

```
0054                *COND FIELD-MAIN CONDITION MUX EQUATES

0056    0000        EQU  LOWER(0)      HARDWIRED FALSE
0057    0001        EQU  UPPER(1)      HARDWIRED TRUE
0058    0002        EQU  AUX1(2)       SELECT LOCAL AUXILIARY CONDITIONS (F1 FIELD)
0059    0003        EQU  FRAEQF(3)     FPA=$F(GOING INTO CURRENT INSTRUCTION)
0060    0004        EQU  AUEQFF(4)     ALU=$FF (AT END OF CURRENT INSTRUCTION)
0061    0005        EQU  FPAEQF(5)     FPA=$F  (GOING INTO CURRENT INSTRUCTION)
0062    0006        EQU  CYNOT(6)      NO CARRY FROM ALU (AT END OF CURRENT INST.)
0063    0007        EQU  RXRDYN(7)     -(RECEIVER HAS DATA READY)

0065                *S1 FIELD-S1 DECODE EQUATES

0067    0001        EQU  N1(1)         NO S-1 INPUT
0068    0001        EQU  L1(1)         LATCH 1
0069    0002        EQU  DFL(2)        DATA FROM MEMORY LOWER
0070    0003        EQU  DFU(3)        DATA FROM MEMORY UPPER
0071    0004        EQU  FLE(4)        FILE
0072    0005        EQU  NAU(5)        -(AQ DATA LOWER)
0073    0006        EQU  NAL(6)        -(AQ DATA LOWER)
0074    0007        EQU  FAD(7)        FILE ADDRESS
0075    0008        EQU  PBXI(8)        PORT BUS/EXTERNAL INTERRUPTS

0077                *ALU FIELD-ALU LOGICAL EQUATES (F1 NE 2 OR 3)

0079    00FF        EQU  NU($FF)       FIELD NOT USED
0080    0000        EQU  S1(0)         S1
0081    0001        EQU  OR(1)         S1+S2
0082    0002        EQU  ORN(2)        S1+(-S2)
0083    0003        EQU  ONES(3)       ONES
0084    0004        EQU  AND(4)        (S1)(S2)
0085    0005        EQU  S2(5)         S2
0086    0006        EQU  EORZ(6)       -(S1 EX. OR S2)
0087    0007        EQU  NOR(7)        -(S1)+S2
0088    0008        EQU  ANDN(8)       (S1)(-S2)
0089    0009        EQU  EOR(9)        S1 EX. OR S2
0090    000A        EQU  S2Z(10)       -S2
0091    000B        EQU  NAND(11)      -((S1)(S2))
0092    000C        EQU  ZERO(12)      ZERO
0093    000D        EQU  NS1AND(13)    -(S1)(S2)
0094    000E        EQU  ORZ(14)       -(S1+S2)
0095    000F        EQU  S1Z(15)       -S1

0097                *ALU FIELD-ALU ARITHMETIC WITHOUT CARRY EQUATES (F1 EQ 2)

0099    0000        EQU  MINUS1(0)     S1 MINUS 1
0100    0003        EQU  SHIFT(3)      S1 PLUS S1 (SHIFT LEFT 1)
0101    0006        EQU  PLUS(6)       S1 PLUS S2
```

```
0103            *ALU FIELD-ALU ARITHMETIC WITH CARRY EQUATES (F1 EQ 3)

0105    0006        EQU  PS2P1(6)      S1 PLUS S2 PLUS 1
0106    0009        EQU  MINUS(9)      S1 MINUS S2
0107    000F        EQU  PLUS1(15)     S1 PLUS 1


0109            *S2 FIELD-S2 FIELD EQUATES

0111    0000        EQU  L2(0)         LATCH 2
0112    0001        EQU  CST(1)        CONSTANT (CONTROL MEMORY BITS 0-7)
0113    0002        EQU  QFL(2)        AQ ADDRESS LOWER
0114    0003        EQU  BTG(3)        BIT GENERATOR (BIT ADDRESS SPECIFIED BY F1)


0116            *DEST FIELD-DESTINATION DECODE EQUATES

0118    0000        EQU  NONE(0)       NO DESTINATION
0119    0001        EQU  ATU(1)        AQ DATA UPPER
0120    0002        EQU  ATL(2)        AQ DATA LOWER
0121    0003        EQU  FA(3)         FILE ADDRESS
0122    0004        EQU  PORTDL(4)     PORT DATA LATCH
0123    0005        EQU  TL1(5)        LATCH 1
0124    0006        EQU  TL2(6)        LATCH 2
0125    0007        EQU  L2F(7)        LATCH 2 AND FILE


0127            *E1AND E2 FIELDS-ENABLE FIELD EQUATES


0129    0000        EQU  EN(0)         ENABLE NEITHER F1 OR F2
0130    0001        EQU  E2(1)         ENABLE F2
0131    0002        EQU  E1(2)         ENABLE F1
0132    0003        EQU  EB(3)         ENABLE BOTH F1 AND F2
```

```
0134                *F1 FIELD-AUXILIARY CONDITION MUX (AUX1) EQUATES

0136    0000            EQU  NSCHER(0)      NO STOP ON CHAN ERR JUMPER
0137    0001            EQU  T1PWA0(1)      TYPE 1 PWA,S ONLY (HI) JUMPER
0138    0002            EQU  PRIT2(2)       PRIMARY PWA IS TYPE 2 (LO) JUMPER
0139    0003            EQU  EXTT2(3)       EXTERNAL PWA IS TYPE 2 (LO) JUMPER
0140    0004            EQU  PPNOT(4)      NOT PROGRAM PROTECT
0141    0005            EQU  READ(5)       AQ READ
0142    0006            EQU  L2BIT0(6)     L2 BIT 0 (BEFORE SHIFT, IF SHIFTING ALSO)
0143    0007            EQU  L2BIT7(7)     L2 BIT 7 (BEFORE SHIFT, IF SHIFTING ALSO)
0144    0008            EQU  DMAFLG(8)     DMA FLAG (DMA FINISHED)
0145    0009            EQU  AQRDWT(9)     AQ FLAG (AQ READ OR WRITE)
0146    000A            EQU  SEGEQ3(10)    SEGMENT EQUAL 3
0147    000B            EQU  DSRSET(11)    DSR/DCD MUX SET TO DSR
0148    000C            EQU  TXRDY(12)     A TRANSMITTER NEEDS DATA
0149    000D            EQU  NOTERR(13)    NOT MEMORY ERROR--NOT(MPE+MPF+MAE)
0150    000E            EQU  MPF(14)       MEMORY PROTECT FAULT
0151    000F            EQU  MAE(15)       MEMORY ADDRESS ERROR

0153                *F1 FIELD- BIT GENERATOR EQUATES

0155    0000            EQU  BG0(0)        SELECT BIT GENERATOR BIT 0
0156    0001            EQU  BG1(1)        SELECT BIT GENERATOR BIT 1
0157    0002            EQU  BG2(2)        SELECT BIT GENERATOR BIT 2
0158    0003            EQU  BG3(3)        SELECT BIT GENERATOR BIT 3
0159    0004            EQU  BG4(4)        SELECT BIT GENERATOR BIT 4
0160    0005            EQU  BG5(5)        SELECT BIT GENERATOR BIT 5
0161    0006            EQU  BG6(6)        SELECT BIT GENERATOR BIT 6
0162    0007            EQU  BG7(7)        SELECT BIT GENERATOR BIT 7

0164                *F1 FIELD-F1 ENABLE EQUATES

0166    0000            EQU  LOADFA(0)      LOAD FILE ADDRESS REGISTER
0167    0001            EQU  CLRERR(1)     CLEAR DMA PROT. FLT., P.E., ADDRESS ERROR
0168    0002            EQU  ARITHN(2)     ALU ARITHMETIC WITHOUT CARRY IN
0169    0003            EQU  ARITHC(3)     ALU ARITHMETIC WITH CARRY IN
0170    0004            EQU  INCFPA(4)      INCREMENT FILE PAGE ADDRESS
0171    0005            EQU  INCTFA(5)      INCREMENT FILE ADDRESS
0172    0006            EQU  SFTL2R(6)     SHIFT L2 RIGHT, INCREMENT FILE ADDRESS
0173    0007            EQU  SFTL2L(7)     SHIFT L2 LEFT, INCREMENT FILE ADDRESS

0175                *F1 FIELD-F1 STROBE EQUATES

0177    0008            EQU  REQDMA(8)     SET REQUEST DMA
0178    0009            EQU  CLRDMA(9)     CLEAR DMA FLAG
0179    000A            EQU  RPLYAQ(10)    SET AQ REPLY
0180    000B            EQU  RJCTAQ(11)    SET AQ REJECT
0181    000C            EQU  STBCB1(12)    STROBE SELECTED CONTROL BITS 1
0182    000D            EQU  CLRUDC(13)     CLEAR THE UP/DOWN COUNTER
0183    000E            EQU  SETDMA(14)    FORCE SET DMA FLAG
0184    000F            EQU  LOPNR(15)     LOAD PORT NUMBER REGISTER FROM THE ALU OUTPUT
```

```
0186                *F2 FIELD-F2 ENABLE EQUATES

0188    0000            EQU  LDFA1(0)       LOAD FILE ADDRESS REGISTER (LOADFA)
0189    0001            EQU  LDDMAH(1)     LOAD DMA ADDRESS HIGH BITS
0190    0002            EQU  LDDTL(2)      LOAD DMA DATA LOWER
0191    0003            EQU  LDDTU(3)      LOAD DMA DATA UPPER
0192    0004            EQU  PEPNR(4)       ENABLE PRIORITY ENCODER OUTPUT TO PNR
0193    0005            EQU  INCFA1(5)      INCREMENT FILE ADDRESS (INCTFA)
0194    0006            EQU  LDDMAL(6)     LOAD DMA ADDRESS LOWER
0195    0007            EQU  LDDMAU(7)     LOAD DMA ADDRESS UPPER


0197                *F2 FIELD-F2 STROBE EQUATES

0199    0008            EQU  ROMPG0(8)     SEL ROM PAGE 0 ON NEXT JPT OR XFM
0200    0009            EQU  ROMPG1(9)     SEL ROM PAGE 1 ON NEXT JPT OR XFM
0201    000A            EQU  SETTM(10)      SET TEST MODE
0202    000B            EQU  PLDUDC(11)     LOAD UP/DOWN COUNTER (SEG NO) FROM F3 FIELD
0203    000C            EQU  LDPCR(12)      LOAD PORT CONTROL REGISTER FROM F3 FIELD
0204    000D           EQU  CNTDWN(13)      DECREMENT UP/DOWN COUNTER (SEG NO)
0205    000E           EQU  CNTUP(14)       INCREMENT UP/DOWN COUNTER (SEG NO)
0206    000F           EQU RSTPEL(15)       RESET PRIORITY ENCODER LATCH FOR NEXT RXPDY


0208                *F2 FIELD-CONTROL BIT 1 EQUATES

0210    0000            EQU  CLRRD(0)       CLEAR DMA READ
0211    0001            EQU  CLRPRT(1)      CLEAR DMA PROTECT
0212    0002            EQU  SELDCD(2)       SELECT DCD MUX INPUTS
0213    0003            EQU  MAB201(3)    IF DMA-MAB20=1
0214    0004            EQU PRTDDS(4)       PORT DATA DISABLE
0215    0005            EQU  MAB181(5)    IF DMA-MAB18=1
0216    0006            EQU  CLRBRG(6)       DROP BRG STROBE
0217    0007           EQU  CLRINT(7)        CLEAR PROGRAM INTERRUPT
0218    0008            EQU  SETRD(8)       SET DMA READ
0219    0009            EQU  SETPRT(9)      SET DMA PROTECT
0220    000A            EQU  SELDSR(10)      SELECT DSR MUX INPUTS
0221    000B            EQU  MAB200(11)   IF DMA-MAB20=0
0222    000C            EQU  PRTDEN(12)     PORT DATA ENABLE
0223    000D            EQU  MAB180(13)   IF DMA-MAB18=0
0224    000E            EQU  SETBRG(14)      RAISE BRG STROBE
0225    000F            EQU  SETINT(15)      SET PROGRAM INTERRUPT
```

```
0227  ****************************************************************************
0228  ** REGISTER FILE MAP, TYPICAL ONE PORT/PAGE (ONE FOR EACH OF 16 PORTS)**
0229  ****************************************************************************

0231  *      SEG 0      *      SEG 1      *      SEG 2      *      SEG 3      *
0232  ***********************************************************************
0233  *                 *                 *                 *                 * F
0234  ***********************************************************************
0235  *                 *                 * TERM STAT WD-U  * TERM STAT WD-L  * E
0236  ***********************************************************************
0237  *                 *  EXT STAT WD    *                 *    MD-FWA-U     * D
0238  ***********************************************************************
0239  *                 *                 * 0 0 0 0MD-FWA-H*    MD-FWA-L     * C
0240  ***********************************************************************
0241  *    R2 FLAGS     *                 *                 *    MS-FWA-U     * B
0242  ***********************************************************************
0243  *    EOT 10       *                 * 0 0 0 0MS-FWA-H*    MS-FWA-L     * A
0244  ***********************************************************************
0245  *    EOT 9        * LAST USART CMD  *     M-CTR-U     *                 * 9
0246  ***********************************************************************
0247  *    EOT 8        *                 *     M-CTR-L     *                 * 8
0248  ***********************************************************************
0249  *    EOT 7        *     T-LEN-U     *     T-LEN-L     *     T-FWA-U     * 7
0250  ***********************************************************************
0251  *    EOT 6        *                 *0 0 0 0 T-FWA-H *     T-FWA-L     * 6
0252  ***********************************************************************
0253  *    EOT 5        *     T1 FLAGS    *     T-CTR-U     *     T-DATA-U    * 5
0254  ***********************************************************************
0255  *    EOT 4        *                 *     T-CTR-L     *     T-DATA-L    * 4
0256  ***********************************************************************
0257  *    EOT 3        *     R-LEN-U     *     R-LEN-L     *     R-FWA-U     * 3
0258  ***********************************************************************
0259  *    EOT 2        * READ DATA HOLD  * 0 0 0 0 R-FWA-H*     R-FWA-L     * 2
0260  ***********************************************************************
0261  *    EOT 1        *     R1 FLAGS    *     R-CTR-U     *     R-DATA-U    * 1
0262  ***********************************************************************
0263  * F 0 0 0 N N N N*RCV DATA U/L FLG*     R-CTR-L     *     R-DATA-L    * 0
0264  ***********************************************************************
0265  *FLAG(F),INDEX(N)* 00=UPPR,FF=LWR *

0267  *                                  ******************
0268  *            R1, T1, R2 FLAG BITS:  * 7 6 5 4 3 2 1 0*
0269  *                                  ******************
0270  *BIT** R1 FLAG DEFINITIONS * T1 FLAG DEFINITIONS * R2 FLAG DEFINITIONS *
0271  ***************************************************************************
0272  * 0 ** DO ECHOPLEX(IF 1 ON)* DATA AVAIL(FROM DMA)* RCVR NEEDS DMA         *
0273  * 1 ** DO ECHO(IF 0 NOT ON)* INSERT LF FOLL CR   * TMTR NEEDS DATA       *
0274  * 2 ** DATA READY FOR ECHO * TERMINATE BLOCK MOVE* BMV RD NEEDS DMA      *
0275  * 3 ** TERMINATE ECHOPLEX  * DATA NOT AVAIL YET  * BMV PRIORITY VS TMTR*
0276  * 4 ** (NOT USED)          * TMT DATA U/L-0=U,1=L* (NOT USED)           *
0277  * 5 ** RCV BUFFER AVAILIBLE* DO CR/LF PREFIX     * (NOT USED)           *
0278  * 6 ** (NOT USED)          * (NOT USED)          * (NOT USED)           *
0279  * 7 ** LOOP-BACK MODE INDIC* TMT TERMINATE       * RCV TERMINATE        *
```

```
0281                    S       CMA+ LOWER,N1,S2,CST,PORTDL,E1,STBCB1,SETBRG,NU  RST PRT(9600 B)
0281 P0000 0000
0281 P0001 80A3
0281 P0002 2CEF
0282                            SEQ  LOWER,N1,ZERO,NU,FA,EB,CLRUDC,LDPCR,$0  SEG=0,LBT OFF BIT
0282 P0003 C3E6
0282 P0004 F0C0
0283                            SEQ+ FPAEQF,NU,NU,NU,NONE,EB,INCFPA,SETTM,NU FRA=F TO GET HERE
0283 P0005 0001
0283 P0006 EFFE
0283 P0007 34AF
0284                    ZTF     CMA  FRAEQF,N1,ZERO,NU,L2F,E1,INCTFA,NU,NU   WRITE ZERO TO FRA
0284 P0008 98E7
0284 P0009 E5FF
0285                            SEQ+ AUX1,NU,NU,NU,NONE,E2,SEGEQ3,CNTUP,NU   FPA=F TO GET HERE
0285 P000A 0002
0285 P000B D7FE
0285 P000C 1AEF
0286                            JPT  LOWER,FAD,S1,NU,FA,E1,LDPNR,ZTF         FPA NOT F
0286 P000D 4386
0286 P000E EF01
0287                            SEQ+ UPPER,N1,ONES,NU,FA,EB,CLRUDC,RSTPEL,NU FA OF STK PTR
0287 P000F 0003
0287 P0010 C89E
0287 P0011 F0FF
0288                            JPT  LOWER,FAD,S1,NU,FA,E1,LDPNR,ZTF         SEG NOT 3
0288 P0012 4386
0288 P0013 EF01
0289                            CMA+ LOWER,NU,NU,NU,NONE,E1,STBCB1,CLRBRG,NU BRGST/PRT RST OFF
0289 P0014 0004
0289 P0015 87FE
0289 P0016 2C6F
0290                            SEQ  UPPER,N1,S2,CST,L2F,E1,SETDMA,$FD       INITIAL STK ADDR
0290 P0017 C8A8
0290 P0018 EEFD
0291                            CMA+ LOWER,NU,NU,NU,NONE,E1,STBCB1,MAB180,NU SET INT BANK
0291 P0019 0005
0291 P001A 87FE
0291 P001B 2C0F
0292                            SEQ  UPPER,N1,ZERO,NU,TL2,E1,STBCB1,MAB200,NU  SET INT BANK
0292 P001C C8E7
0292 P001D AC8F
0293                    MCMODE  CMA+ LOWER,N1,S2,CST,PORTDL,E1,CLRERR,$7A     BEG MDE TO URT RTN
0293 P001E 0006
0293 P001F 80A8
0293 P0020 217A
0294                            SEQ  UPPER,N1,ZERO,NU,FA,E1,STBCB1,PRTDEN,NU PDL ON
0294 P0021 C8E6
0294 P0022 ECCF
0295                    NXTPRT  CMA+ LOWER,FAD,S1,NU,FA,EB,LDPNR,LDPCR,$1    SELECT PORT
0295 P0023 0007
0295 P0024 8336
0295 P0025 FFC1
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0296                        SEQ  UPPER,NU,NU,NU,NONE,E2,NU,LDPCR,$9       CS-WR-CMD
0296 P0026 CFFE
0296 P0027 1FC9
0297                        CMA+ LOWER,N1,S2,CST,TL1,E1,INCFPA,NXTPRT/N-S/N  INCR PRT NO
0297 P0028 0008
0297 P0029 80AB
0297 P002A 6407
0298                        SEQ  AUEQFF,FAD,S1Z,NU,NONE,E2,NU,LDPCR,$0    CS-WR OFF
0298 P002B E3FE
0298 P002C 1FC0
0299                        SEQ+ AUEQFF,N1,S2Z,L2,TL2,E1,STBCB1,PRTODS,NU  FA=00,DONE
0299 P002D 0009
0299 P002E E001
0299 P002F AC4F
0300                        XFM  UPPER,L1,S1,NU,NONE,E1,STBCB1,SETPRT,NU  SET M-PROT,LOOP
0300 P0030 0886
0300 P0031 2C9F
0301                        JPT+ LOWER,N1,S2,BTG,PORTDL,EN,BG4,MCMODE     MC URT COMMAND
0301 P0032 000A
0301 P0033 40AF
0301 P0034 0406
0302                INTOFF  SEQ  UPPER,NU,NU,NU,NONE,E1,STBCB1,CLRINT,NU
0302 P0035 CFFE
0302 P0036 2C7F
0303                AQSCAN  CMA+ LOWER,N1,S2,CST,TL1,EN,NU,$07             00000111 TO L1
0303 P0037 0008
0303 P0038 80AB
0303 P0039 4F07
0304                        SEQ  AUX1,L1,NS1AND,QFL,TL2,E2,AQRDWT,PLDUDC,$0  GET 0PPPP000
0304 P003A 00ED
0304 P003B 99B0
0305                        SEQ+ UPPER,L1,AND,QFL,TL1,E1,SFTL2L,NU,NU     HERE IF AQ
0305 P003C 000C
0305 P003D C8A5
0305 P003E 67FF
0306                        JPT  RXRDYN,L1,PLUS,BTG,TL2,E1,ARITHN,RXRDY1 GO TO RXRDY(L2=0B)
0306 P003F 7837
0306 P0040 A232
0307                        CMA+ LOWER,N1,S2,L2,FA,EB,LDPNR,CNTUP,NU      PNR SETFRAG SEG1
0307 P0041 0000
0307 P0042 80A8
0307 P0043 FFEF
0308                        SEQ  AUX1,N1,ZERO,NU,ATU,E2,READ,LOADFA,$0     TEST FOR READ
0308 P0044 00E6
0308 P0045 5500
0309                        XFM+ UPPER,L1,PLUS,CST,NONE,E1,ARITHN,AQJMT/N-S/N *GO TO JMP TABL
0309 P0046 000E
0309 P0047 0832
0309 P0048 2210
0310                        SEQ  AUX1,NU,NU,NU,NONE,EN,PPNOT,NU,NU        HERE IF WRITE
0310 P0049 07FE
0310 P004A 04FF
0311                        JPT+ UPPER,NU,NU,NU,NONE,E1,RJCTAQ,AQSCAN     NOT PROT REJECT
```

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0311 P0048 000F
0311 P0049 4FFE
0311 P004A 2B0B
0312                    XFM   LOWER,L1,PLUS,CST,NONE,E1,ARITHN,AQJMT/N-S/N *GO TO JMP TABL
0312 P004B 0082
0312 P004C 2210
0313                AQJMT JPT+ UPPER,N1,ONES,NU,FA,E1,CLRUDC,TSR        TERM SR
0313 P004D 0010
0313 P004E 489E
0313 P004F ED21
0314                    JPT   AUEQFF,NAL,ORN,BTG,NONE,EN,BG3,PRTMDS    PORT MODE,LWR IF MC
0314 P0050 6316
0314 P0051 0327
0315                    JPT+ UPPER,N1,S2,QFL,TL1,EN,NU,RBCNT           RCV BYTE CNT SR
0315 P0052 0011
0315 P0053 48AD
0315 P0054 4F74
0316                    JPT   UPPER,NAU,S1Z,NU,TL1,EN,NU,RFWA16        RCV FWA, GET AU
0316 P0055 4AFF
0316 P0056 4F98
0317                    JPT+ UPPER,FAD,OR,BTG,FA,EN,BG2,TBCNT          TMT BYTE CNT SR
0317 P0057 0012
0317 P0058 438E
0317 P0059 C274
0318                    JPT   UPPER,NAU,S1Z,NU,TL1,EN,NU,TFWA16        TMT FWA, GET AU
0318 P005A 4AFF
0318 P005B 4F9C
0319                    JPT+ UPPER,FAD,S1,NU,ATU,EN,NU,EXTSWR          EXT SR
0319 P005C 0013
0319 P005D 4886
0319 P005E 4F78
0320                    JPT   UPPER,NAU,S1Z,NU,TL1,EN,NU,MFWA16        MV FWA, GET AU
0320 P005F 4AFF
0320 P0060 4F9A
0321                    JPT+ UPPER,FAD,S1,NU,ATU,E1,INCTFA,CTSDSR      CTS DIAG SR
0321 P0061 0014
0321 P0062 4886
0321 P0063 651A
0322                    JPT   UPPER,NAL,S1Z,NU,TL1,EN,NU,SUBFUN        AL TO L1
0322 P0064 487F
0322 P0065 4F79
0323                    JPT+ UPPER,N1,S2,CST,TL2,EN,NU,AQEC01
0323 P0066 0015
0323 P0067 48AB
0323 P0068 8F18
0324                    JPT   AUEQFF,NAL,S1,NU,TL1,EN,NU,RLEN          RCV LEN, TEST NAL
0324 P0069 6307
0324 P006A 4F90
0325                    JPT+ UPPER,N1,ZERO,NU,ATL,E1,RPLYAQ,EOTLT      FORCE R-TERM
0325 P006B 0016
0325 P006C 43E6
0325 P006D AA36
0326                    JPT   AUEQFF,NAL,S1,NU,TL1,EN,NU,TLEN          TMT LEN, TEST NAL
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0326 P0071 6307
0326 P0072 4FA0
0327                SPSTRD JPT+ UPPER,PBXI,S1Z,NU,ATL,E1,RPLYAQ,AQSCAN  SPECIAL SR-COMPLETE
0327 P0073 0017
0327 P0074 4C7E
0327 P0075 AA0B
0328                       JPT  AUEQFF,NAL,S1,NU,TL2,EN,NU,MLEN          MV LEN,TEST NAL
0328 P0076 6307
0328 P0077 8FAB
0329                AQEC01 CMA+ LOWER,N1,S2,L2,PORTDL,E8,STBCB1,LDPCR,$4  RD ON-EN PDL
0329 P0078 0018
0329 P0079 80A9
0329 P007A 3CC4
0330                       SEQ  UPPER,PBXI,S1,NU,FA,E2,NU,LDPCR,$0        RD OFF
0330 P007B CC06
0330 P007C 0FC0
0331                       CMA+ LOWER,FAD,ORN,L2,ATU,E1,STBCB1,PRTODS,NU  FF TO AL
0331 P007D 0019
0331 P007E 8390
0331 P007F 6C4F
0332                       JPT  UPPER,N1,ZERO,NU,ATL,E1,RPLYAQ,AQSCAN
0332 P0080 48E6
0332 P0081 AA0B
0333                CTSDSR SEQ+ AUEQFF,FLE,ORN,BTG,NONE,E2,BG7,LDPCR,$1 CS-STATUS
0333 P0082 001A
0333 P0083 E216
0333 P0084 17C1
0334                       XFM  UPPER,L1,S1,NU,NONE,E2,NU,LDPCR,$0       CTRLS OFF
0334 P0085 0886
0334 P0086 1FC0
0335                       SEQ+ UPPER,NU,NU,NU,NONE,E2,NU,LDPCR,$5       CS-RD-ST
0335 P0087 0018
0335 P0088 CFFE
0335 P0089 1FC5
0336                       CMA  UPPER,FAD,S1,NU,ATU,EN,NU,NU,NU          NOT IN LBT MDE
0336 P008A 8886
0336 P008B 4FFF
0337                       CMA+ LOWER,N1,S2,CST,TL1,EN,NU,AQSCAN/N-S/N   NOP
0337 P008C 001C
0337 P008D 80AB
0337 P008E 4F0B
0338                       JPT  LOWER,PBXI,S1,NU,ATL,E1,RPLYAQ,CTSDSR
0338 P008F 4406
0338 P0090 AA1A
```

```
0340                ****** FAD=PPPP1110 TO ENTER, POSTED FRA=E; POINTERS AT FRA=D ******
0341                STKSTW CMA+ LOWER,FAD,S1,NU,TL1,E1,CLRUDC,NU,NU     FRA OF POSTED FLAG
0341 P0091 001D
0341 P0092 8387
0341 P0093 60FF
0342                       XFM  UPPER,FLE,PLUS,CST,NONE,E1,ARITHN,POST/N-S/N  DONE IF POSTED
0342 P0094 CA32
0342 P0095 221E
0343                POST   CMA+ LOWER,N1,S2,CST,L2F,EN,NU,$02           SET POSTED FLAG
0343 P0096 001E
0343 P0097 80AB
0343 P0098 CF02
0344                       SEQ  UPPER,N1,ONES,NU,FA,EN,NU,NU,NU         STK PTR ADDR
0344 P0099 C89E
0344 P009A CFFF
0345                       CMA+ LOWER,FLE,MINUS,CST,L2F,E1,ARITHC,$10   DECR TO NEXT STK LOC
0345 P009B 001F
0345 P009C 8248
0345 P009D E310
0346                       SEQ  LOWER,N1,S2,L2,FA,E1,STBCB1,SETINT,NU   NEXT TO FA
0346 P009E C0A8
0346 P009F ECFF
0347                       JPT+ UPPER,NU,NU,NU,NONE,EN,NU,AQSCAN
0347 P00A0 0020
0347 P00A1 4FFE
0347 P00A2 0F08
0348                       CMA  UPPER,L1,S1,NU,L2F,E1,INCFPA,NU,NU      BACK UP BY 1-STORE
0348 P00A3 8887
0348 P00A4 E4FF
0349                TSR    SEQ+ AUEQFF,FLE,OR,BTG,NONE,EN,BG1,NU,NU     TEST FOR 11111101
0349 P00A5 0021
0349 P00A6 E20E
0349 P00A7 01FF
0350                       JPT  AUEQFF,FLE,S1Z,NU,NONE,E1,INCTFA,NIPTST TST FE FOR 00
0350 P00A8 627E
0350 P00A9 25FE
0351                       JPT+ LOWER,N1,S2Z,BTG,FA,EN,BG0,TSR              END OF STACK
0351 P00AA 0022
0351 P00AB 40D6
0351 P00AC C021
0352                TSRSF  SEQ  UPPER,FLE,PLUS,CST,L2F,E1,ARITHN,$10     HERE-STATUS,PTR LOC
0352 P00AD CA33
0352 P00AE E210
0353                       CMA+ LOWER,N1,S2,L2,FA,EN,NU,NU,NU           SW PTR TO FA
0353 P00AF 0023
0353 P00B0 80A8
0353 P00B1 CFFF
0354                       SEQ  UPPER,FLE,S1,NU,FA,E2,NU,CNTDWN,NU      SW FA TO FAD,SEG3
0354 P00B2 CA06
0354 P00B3 0F0F
0355                       CMA+ LOWER,FLE,S1,NU,ATL,E2,NU,CNTDWN,NU     SW L-SEG3, TO SEG2
0355 P00B4 0024
0355 P00B5 8256
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0355 P00B6 9FDF
0356                    SEQ  UPPER,FAD,AND,CST,TL2,EN,NU,$F0          MASK FPA TO L2
0356 P00B7 CBA3
0356 P00B8 8FF0
0357                    CMA+ LOWER,FLE,OR,L2,ATU,EB,RPLYAQ,PLDUDC,$3 TO SEG 3
0357 P00B9 0025
0357 P00BA 8208
0357 P00BB 7A33
0358                    SEQ  UPPER,FLE,AND,CST,L2F,EN,NU,$06        CLR ST WD,EXCPT MDM
0358 P00BC CA23
0358 P00BD CF06
0359                    CMA+ LOWER,N1,ZERO,NU,L2F,E2,NU,CNTDWN,NU     SEG 2
0359 P00BE 0026
0359 P00BF 80E7
0359 P00C0 0F0F
0360                    JPT  UPPER,N1,ZERO,NU,L2F,E1,CLRUDC,AQSCAN     SEG 0
0360 P00C1 48E7
0360 P00C2 ED03
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0362                 PRTMDS SEQ+ UPPER,NAU,S1Z,NU,TL1,EB,INCTFA,LDPCR,$0 TO FRA1,TM OFF BIT
0362 P00C3 0027
0362 P00C4 CAFF
0362 P00C5 75C0
0363                        JPT  UPPER,NU,NU,NU,NONE,E1,RPLYAQ,S          MASTER CLEAR
0363 P00C6 4FFE
0363 P00C7 2A00
0364                        CMA+ LOWER,FLE,ANDN,CST,L2F,E1,STBCB1,SETBRG,$3  CLR R1 FLAGS
0364 P00C8 0028
0364 P00C9 8243
0364 P00CA ECE3
0365                        SEQ  LOWER,NAL,S1Z,NU,TL2,EB,RPLYAQ,SETTM,NU  CLR LOOP TST
0365 P00CB C37F
0365 P00CC 8AAF
0366                        SEQ+ UPPER,NU,NU,NU,NONE,E1,STBCB1,CLRBRG,NU  DLY COMPL,BD RT SET
0366 P00CD 0029
0366 P00CE CFFE
0366 P00CF 2C6F
0367                        CMA  FRAEQF,N1,S2,L2,PORTDL,E1,INCTFA,NU,NU   URT RST DLY
0367 P00D0 98A9
0367 P00D1 25FF
0368                        CMA+ LOWER,L1,S1,NU,PORTDL,E1,LOADFA,$00      FRA TO R1 FLGS
0368 P00D2 002A
0368 P00D3 8087
0368 P00D4 2000
0369                        SEQ  AUX1,N1,ZERO,NU,TL1,EB,SFTL2R,LDPCR,$2  *TST AND SH L2 LSB
0369 P00D5 00E7
0369 P00D6 76C2
0370                        SEQ+ AUX1,N1,S2,CST,TL2,EN,L2BIT0,$22         HERE IF TST MODE
0370 P00D7 002B
0370 P00D8 00AB
0370 P00D9 8622
0371                 SETDLY JPT  LOWER,N1,S2,BTG,FA,EN,BG2,DELAY          HERE-NORMAL,DLY 12
0371 P00DA 40AE
0371 P00DB C22E
0372                        SEQ+ UPPER,N1,S2,CST,TL1,EN,NU,$37            HERE-ECHO,L1 IS CMD
0372 P00DC 002C
0372 P00DD C8AB
0372 P00DE 4F37
0373                        SEQ  UPPER,N1,S2,BTG,TL2,E2,BG7,SETTM,NU      HERE-LOOP TEST
0373 P00DF C8AF
0373 P00E0 97AF
0374                        JPT+ LOWER,FLE,OR,L2,L2F,EN,NU,SETDLY         SET ECO/LB FLG
0374 P00E1 002D
0374 P00E2 4209
0374 P00E3 CF28
0375                 SETMIP JPT  UPPER,N1,S2,BTG,L2F,EN,BG0,TROFF3        SET MIP FLAG,EXIT
0375 P00E4 484F
0375 P00E5 C068
0376                        SEQ+ UPPER,NU,NU,NU,NONE,EB,STBCB1,LDPCR,$1   CS-WR-POL EN
0376 P00E6 002E
0376 P00E7 CFFE
0376 P00E8 3CC1
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0377                DELAY  CMA   FRAEQF,NU,NU,NU,NONE,E1,INCTFA,NU,NU     DELAY
0377 P00E9 9FFE
0377 P00EA 25FF
0378                       CMA+  LOWER,NU,NU,NU,NONE,E2,NU,LDPCR,$9       CS-CMD-WR
0378 P00EB 002F
0378 P00EC 87FE
0378 P00ED 1FC9
0379                       SEQ   UPPER,NU,NU,NU,NONE,EN,NU,NU,NU          NOP
0379 P00EE CFFE
0379 P00EF 0FFF
0380                       CMA+  LOWER,NU,NU,NU,NONE,E2,NU,LDPCR,$0       CS-WR OFF
0380 P00F0 0030
0380 P00F1 87FE
0380 P00F2 1FC0
0381                       SEQ   AUX1,L1,S1,NU,PORTDL,E2,SEGEQ3,PLOUDC,$3  TEST FOR LOOP
0381 P00F3 0087
0381 P00F4 1AB3
0382                       JPT+  LOWER,N1,ONES,NU,FA,EN,NU,SETMIP         SEG EQ 3,SET MIP
0382 P00F5 0031
0382 P00F6 409E
0382 P00F7 CF2D
0383                       JPT   LOWER,NU,NU,NU,NONE,EN,NU,SETDLY      SEG NOT 3,LOOP FOR CMD
0383 P00F8 47FE
0383 P00F9 0F2B
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0385                RXRDY1 JPT+ AUX1,NU,NU,NU,NONE,EN,DMAFLG,DMAFL1      NO RCVR HAS DATA
0385 P00FA 0032
0385 P00FB 57FE
0385 P00FC 0883
0386
                           SEQ  UPPER,NU,NU,NU,NONE,EB,LDPNR,PEPNR,NU    SET PNR
0386 P00FD CFFE
0386 P00FE 3F4F
0387
                           CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,CNTUP,$2   FRA2,SEG1,PNR SET
0387 P00FF 0033
0387 P0100 87FE
0387 P0101 30E2
0388
                           SEQ  UPPER,FLE,S1,NU,TL1,EB,LOADFA,PLDUDC,$0  DATA TO L1,FA OF EOT
0388 P0102 CA07
0388 P0103 7080
0389
                           SEQ+ AUEQFF,FLE,OR,CST,NONE,EN,NU,$7F         TEST EOT FLAG
0389 P0104 0034
0389 P0105 E20A
0389 P0106 0F7F
0390                EOTHI  JPT  UPPER,FAD,OR,L2,FA,EN,NU,EOTCMP          FA TO HI ORDER EOT
0390 P0107 4888
0390 P0108 CF38
0391
                           JPT+ LOWER,FLE,EOR,BTG,L2F,EN,BG7,EOTHI       FLG WAS ON,SET OFF
0391 P0109 0035
0391 P010A 424F
0391 P010B C734
0392
                           JPT  LOWER,FAD,OR,L2,FA,EN,NU,MOETST          FRA=B,TST R-DMA REQ
0392 P010C 4388
0392 P010D CFA0
0393                EOTLT  JPT+ UPPER,N1,S2Z,BTG,TL1,EN,BG1,EOTRLT       EOTHIT
0393 P010E 0036
0393 P010F 4807
0393 P0110 4149
0394
                           SEQ  AUEQFF,FAD,NAND,CST,NONE,EN,NU,$0E       TEST FOR LOOP
0394 P0111 E30A
0394 P0112 0F0E
0395
                           JPT+ UPPER,NU,NU,NU,NONE,EN,NU,AQSCAN         FA=PPPP0001-CONE
0395 P0113 0037
0395 P0114 4FFE
0395 P0115 0F0B
0396
                           SEQ  LOWER,FAD,MINUS1,NU,FA,E1,ARITHN,NU,NU   DCR FA
0396 P0116 C386
0396 P0117 E2FF
0397                EOTCMP CMA+ LOWER,L1,S1,NU,TL2,E2,NU,RSTPEL,NU        DATA-L1 TO L2
0397 P0118 0038
0397 P0119 8087
0397 P011A 9FFF
0398
                           JPT  AUEQFF,FLE,EORZ,L2,NONE,EN,NU,EOTLT      COMPARE EOT
0398 P011B 6230
0398 P011C 0F36
0399                RDURT  CMA+ LOWER,NU,NU,NU,NONE,EB,CLRUDC,LDPCR,$3   CS-CD, SEG00
0399 P011D 0039
0399 P011E 87FE
0399 P011F 30C3
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0400                        SEQ  UPPER,NU,NU,NU,NONE,E2,NU,LDPCR,$7       CS-CD-RD
0400 P0120 CFFE
0400 P0121 1FC7
0401                        CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,CNTUP,$2  SEG1, FRA2
0401 P0122 003A
0401 P0123 87FE
0401 P0124 30E2
0402                        SEQ  UPPER,PBXI,S1,NU,L2F,E2,NU,LDPCR,$1     DATA TO FILE,RD OFF
0402 P0125 CC07
0402 P0126 0FC1
0403                        CMA+ LOWER,N1,S2,L2,TL1,E1,LOADFA,$01        DATA-L1,FRA1,SEG1
0403 P0127 003B
0403 P0128 80A9
0403 P0129 6001
0404                        SEQ  AUEQFF,FLE,NOR,CST,NONE,EN,NU,$DF       CK RBA FLAG
0404 P012A E23A
0404 P012B 0F0F
0405                        JPT+ UPPER,N1,S2Z,BTG,TL2,EN,BG2,RCVDIS      FLAG OFF-DIS RCVR
0405 P012C 003C
0405 P012D 4807
0405 P012E 8252
0406                        SEQ  AUEQFF,FLE,ORN,BTG,NONE,EN,BG1,NU,NU    CK ECHO FLAG-FRA1
0406 P012F E216
0406 P0130 01FF
0407                        JPT+ UPPER,NU,NU,NU,NONE,EN,NU,ECOFLG        IS ECHO MODE
0407 P0131 003D
0407 P0132 4FFE
0407 P0133 0F4C
0408                RXSTAT  SEQ  UPPER,NU,NU,NU,NONE,EB,CLRUDC,LDPCR,$5  NOT E.MDE,CS-CD,RD
0408 P0134 CFFE
0408 P0135 3DC5
0409                        CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,CNTDWN,$E  FRA-E,SEG3-ST WRD
0409 P0136 003E
0409 P0137 87FE
0409 P0138 30DE
0410                        SEQ  UPPER,PBXI,AND,CST,TL2,EN,NU,$38        STATUS-L2(FE,OE,PE)
0410 P0139 CC23
0410 P013A 8F38
0411                        CMA+ LOWER,FLE,OR,L2,L2F,EN,NU,NU,NU         URT ER STATUS TO FLE
0411 P013B 003F
0411 P013C 8209
0411 P013D CFFF
0412                        SEQ  UPPER,N1,ZERO,NU,L2F,EB,LOADFA,LDPCR,$0 URT CTLS OFF, FRA0
0412 P013E C8E7
0412 P013F F0C0
0413                        CMA+ LOWER,NU,NU,NU,NONE,E2,NU,PLDUDC,$1     SEG1,FRA0
0413 P0140 0040
0413 P0141 87FE
0413 P0142 1F81
0414                        SEQ  AUEQFF,FLE,EOR,CST,L2F,EN,NU,$FF        TEST/FLIP U/L,FRA2
0414 P0143 E24B
0414 P0144 CFFF
0415                        SEQ+ UPPER,FAD,OR,BTG,FA,E2,BG0,PLDUDC,$3    UPPER DATA,FRA1,SEG3
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0415 P0145 0041
0415 P0146 CB8E
0415 P0147 0083
0416                    SEQ  UPPER,NU,NU,NU,NONE,E2,NU,PLDUDC,$3      LOWER DATA,FRA0,SEG3
0416 P0148 CFFE
0416 P0149 1F83
0417                    JPT+ AUX1,L1,S1,NU,L2F,EN,NSCHER,CHERJP      DATA TO FILE,SEG3
0417 P014A 0042
0417 P014B 5087
0417 P014C C0FF
0418                CERTST SEQ  UPPER,N1,ONES,NU,TL1,E1,LOADFA,$0E   SEG3, FRA E
0418 P014D C89F
0418 P014E 600E
0419                    CMA+ LOWER,N1,S2,CST,TL2,EN,NU,EOTRLT/N-S/N  ERROR EXIT ADDR
0419 P014F 0043
0419 P0150 80AB
0419 P0151 8F49
0420                    SEQ  AUEQFF,FLE,NOR,CST,NONE,EN,NU,$CF           *TEST FOR OE,FE
0420 P0152 E23A
0420 P0153 0FCF
0421                NERTST SEQ+ UPPER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$0 NO ERR,SET FRA0,SEG0
0421 P0154 0044
0421 P0155 CFFE
0421 P0156 3080
0422                    XFM  UPPER,N1,S2,L2,NONE,E2,NU,RSTPEL,NU     FE OR OE FOUND,TERM
0422 P0157 08A8
0422 P0158 1FFF
0423                    JPT+ AUEQFF,FLE,S1Z,NU,TL1,EN,NU,EOTFLG      ANY EOTS ACTIVE
0423 P0159 0045
0423 P015A 627F
0423 P015B 4F4B
0424                RLENAD SEQ  UPPER,NU,NU,NU,NONE,E2,NU,PLDUDC,$2  TO FRA0,SEG 2
0424 P015C CFFE
0424 P015D 1F82
0425                CTDNRL SEQ+ CYNOT,FLE,MINUS1,NU,L2F,E1,ARITHN,NU,NU DECR LOWER CTR(SEG2)
0425 P015E 0046
0425 P015F F207
0425 P0160 E2FF
0426                    JPT  LOWER,FLE,MINUS1,NU,L2F,E1,ARITHN,EOTCK DECR UPPER CTR...
0426 P0161 4207
0426 P0162 E248
0427                    JPT+ LOWER,NU,NU,NU,NONE,E1,INCTFA,CTDNRL    BORROW, GET UPPER
0427 P0163 0047
0427 P0164 47FE
0427 P0165 2546
0428                    SEQ  AUEQFF,N1,S2Z,L2,NONE,E1,INCTFA,NU,NU   NO BORROW, ZERO TEST
0428 P0166 E000
0428 P0167 25FF
0429                    SEQ+ AUEQFF,FLE,S1Z,NU,TL1,EB,LOADFA,CNTDWN,$0  CTR-L=0,TST UPPP
0429 P0168 0048
0429 P0169 E27F
0429 P016A 7000
0430                EOTCK  SEQ  LOWER,NU,NU,NU,NONE,EB,LOADFA,CNTDWN,$0 LOWER CTR NOT 0...
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0430 P016B C7BE
0430 P016C 3000
0431                EOTRLT JPT+ LOWER,L1,NOR,BTG,TL2,EN,BG2,RXTERM      BOTH CTR U/L=0, TERM
0431 P016D 0049
0431 P016E 40BF
0431 P016F 824E
0432                       SEQ  AUEQFF,FLE,S1,NU,NONE,EB,CLRUDC,LOADFA,$B *TST U/L-FA TO R2
0432 P0170 E206
0432 P0171 3008
0433                       JPT+ UPPER,NU,NU,NU,NONE,EN,NU,AQSCAN          DMA NOT RQD FLG=FF
0433 P0172 004A
0433 P0173 4FFE
0433 P0174 0F0B
0434                       CMA  UPPER,FLE,OR,BTG,L2F,EN,BG0,NU,NU         DMA RQD       FLG=00
0434 P0175 8A0F
0434 P0176 C0FF
0435                EOTFLG CMA+ LOWER,N1,S2Z,BTG,TL1,E2,BG7,RSTPEL,NU   HERE-NO EOTS,RST PEL
0435 P0177 0048
0435 P0178 80D7
0435 P0179 57FF
0436                       JPT  LOWER,L1,EORZ,BTG,L2F,EN,BG7,RLENAD      HERE-EOTS ACTIVE
0436 P017A 40B7
0436 P017B C745
0437                ECOFLG CMA+ LOWER,FLE,OR,BTG,L2F,EN,BG2,NU,NU       SET DATA-TO-ECHO FLG
0437 P017C 004C
0437 P017D 820F
0437 P017E C2FF
0438                       SEQ  AUX1,N1,S2,CST,TL2,EN,L2BIT0,TROFF3/N-S/N  TST ECOPLX FL L2
0438 P017F 00AB
0438 P0180 9668
0439                       JPT+ LOWER,NU,NU,NU,NONE,EN,NU,RXSTAT         FLAG ON-RETURN
0439 P0181 004D
0439 P0182 47FE
0439 P0183 0F30
0440                       XFM  UPPER,N1,S2,L2,NONE,E2,NU,RSTPEL,NU      NOT ON-EC TEST MDE
0440 P0184 38A8
0440 P0185 1FFF
0441                RLZTRM SEQ+ UPPER,N1,S2,CST,TL1,EN,NU,RCVEND/N-S/N  SET EXIT
0441 P0186 004E
0441 P0187 C8AB
0441 P0188 4FC3
0442                RXTERM SEQ  UPPER,N1,S2,CST,TL1,EN,NU,AQSCAN/N-S/N  SET EXIT
0442 P0189 C8AB
0442 P018A 4F0B
0443                       CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$E ST WD-FRA E,SEG2
0443 P018B 004F
0443 P018C 87FE
0443 P018D 308E
0444                       SEQ  UPPER,FLE,OR,L2,L2F,EN,NU,NU,NU          R STATUS BITS
0444 P018E CA09
0444 P018F CFFF
0445                       CMA+ LOWER,NU,NU,NU,NONE,EB,CLRUDC,LOADFA,$B FLAG R2
0445 P0190 0050
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0445 P0191 87FE
0445 P0192 3008
0446                    SEQ  UPPER,FLE,OR,CST,L2F,EN,NU,$81          R TERM/DMA RQD
0446 P0193 CA0B
0446 P0194 CF81
0447                    CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLOUDC,$1 RBA FLG IN R1
0447 P0195 0051
0447 P0196 87FE
0447 P0197 3081
0448                    JPT  LOWER,FLE,ANDN,BTG,L2F,EN,BG5,RXTXIT    CLR RBA FLAG
0448 P0198 4247
0448 P0199 C55A
0449            RCVDIS  CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLOUDC,$9 FRA9,SEG1
0449 P019A 0052
0449 P019B 87FE
0449 P019C 3089
0450                    SEQ  UPPER,FLE,AND,L2,PORTDL,E1,STBCB1,PRTDEN,NU RXEN OFF
0450 P019D CA21
0450 P019E 2CCF
0451                    CMA+ LOWER,FLE,ANDN,BTG,L2F,E2,BG2,LDPCR,$9   CS-CD-WR
0451 P019F 0053
0451 P01A0 8247
0451 P01A1 02C9
0452                    JPT  UPPER,NU,NU,NU,NONE,EN,NU,RCVOFF        FINISH BELOW
0452 P01A2 4FFE
0452 P01A3 0F67
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0454                TXRDY1 CMA+ LOWER,N1,S2,CST,FA,E1,CLRUDC,$0C        LAST TMTR FA0C,SEG0
0454 P01A4 0054
0454 P01A5 80AA
0454 P01A6 ED0C
0455                       SEQ  UPPER,FLE,PLUS,CST,L2F,E1,ARITHN,$10    INCR TO THIS TMTR
0455 P01A7 CA33
0455 P01A8 E210
0456                       CMA+ LOWER,N1,S2,L2,FA,E1,LDPNR,NU,NU        SET PNR
0456 P01A9 0055
0456 P01AA 80A8
0456 P01AB EFFF
0457                       SEQ  UPPER,NU,NU,NU,NONE,EB,LOADFA,CNTUP,$5  FLAG AT FRA5,SEG1
0457 P01AC CFFE
0457 P01AD 30E5
0458                TLZX   CMA+ LOWER,N1,S2,CST,TL1,EN,NU,TRTRM1/N-S/N  FOR TERM RTN
0458 P01AE 0056
0458 P01AF 80AB
0458 P01B0 4F72
0459                       SEQ  AUEQFF,FLE,NAND,BTG,NONE,EN,BG7,NU,NU   TST TRM FLG
0459 P01B1 E25E
0459 P01B2 07FF
0460                       SEQ+ AUX1,N1,S2,CST,TL2,EN,TXRDY,$04         TERM NOT ON
0460 P01B3 0057
0460 P01B4 D0A3
0460 P01B5 8C04
0461                       JPT  UPPER,NU,NU,NU,NONE,EN,NU,TROFF2        T-TRM FLG ON
0461 P01B6 4FFE
0461 P01B7 0F60
0462                       SEQ+ AUEQFF,FLE,ORN,BTG,NONE,EN,BG0,NU,NU    UART NEEDS DATA
0462 P01B8 0058
0462 P01B9 E216
0462 P01BA 00FF
0463                       JPT  UPPER,NU,NU,NU,NONE,EN,NU,MDMSCN        TMTR NOT RDY,EXIT
0463 P01BB 4FFE
0463 P01BC 0FEF
0464                       SEQ+ UPPER,FLE,S1,NU,TL1,E2,NU,PLOUDC,$3     BUF DATA AV,GET T1
0464 P01BD 0059
0464 P01BE CA07
0464 P01BF 5F83
0465                       JPT  LOWER,FAD,EOR,L2,FA,EN,NU,ECOTMT        BUFF DATA NOT AVAIL
0465 P01C0 43C8
0465 P01C1 0F69
0466                       SEQ+ AUEQFF,L1,ORN,BTG,NONE,E2,BG4,LOADFA,$4 TST U/L,TO FRA4
0466 P01C2 005A
0466 P01C3 E096
0466 P01C4 1404
0467                RXTXIT XFM  UPPER,L1,S1,NU,NONE,EB,CLRUDC,LOADFA,$B RXTERM EXIT (FRA=B)
0467 P01C5 0886
0467 P01C6 3D08
0468                       SEQ+ UPPER,FLE,S1,NU,PORTDL,EB,STBCB1,LDPCR,$4 U/L=1,LWR,FRA4
0468 P01C7 0058
0468 P01C8 CA07
0468 P01C9 3CC4
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0469                        CMA   UPPER,NU,NU,NU,NONE,E1,INCTFA,NU,NU      U/L=0,UPPR,FRA5
0469 P01CA 8FFE
0469 P01CB 25FF
0470                        SEQ+  AUEQFF,L1,ORN,BTG,NONE,EN,BG5,NU,NU      TST CRLF PFX FLG
0470 P01CC 005C
0470 P01CD E096
0470 P01CE 05FF
0471                 INSLF1 JPT   LOWER,L1,OR,BTG,L2F,EN,BG3,DOTMT         LF BITS TO FILE
0471 P01CF 408F
0471 P01D0 0366
0472                        JPT+  LOWER,NU,NU,NU,NONE,EN,NU,FLPTUL         CRLF FLG ON
0472 P01D1 0050
0472 P01D2 47FE
0472 P01D3 0F62
0473                        SEQ   AUEQFF,PBXI,EORZ,CST,NONE,EN,NU,$0D      CRLF FLG NOT ON
0473 P01D4 E432
0473 P01D5 0F00
0474                        SEQ+  AUEQFF,L1,ORN,BTG,NONE,E2,BG1,LDPCR,$0   DATA=CR,TST ILF FLG
0474 P01D6 005E
0474 P01D7 E096
0474 P01D8 11C0
0475                        SEQ   LOWER,NU,NU,NU,NONE,E2,NU,LDPCR,$0       DATA NOT CR
0475 P01D9 C7FE
0475 P01DA 1FC0
0476                        JPT+  LOWER,N1,S2,BTG,TL1,EN,BG1,INSLF1        DATA=CR,ILF ON
0476 P01DB 005F
0476 P01DC 40AF
0476 P01DD 415C
0477                        SEQ   UPPER,NU,NU,NU,NONE,EB,LOADFA,CNTDWN,$4  ILF NOT ON,DCR LEN
0477 P01DE CFFE
0477 P01DF 30D4
0478                        SEQ+  CYNOT,FLE,MINUS1,NU,L2F,E1,ARITHN,NU,NU  FRA4,SEG2,CTR-L
0478 P01E0 0060
0478 P01E1 F207
0478 P01E2 E2FF
0479                 TBRRW  JPT   LOWER,FLE,MINUS1,NU,L2F,E1,ARITHN,FLPTUL  DCR CTR-U
0479 P01E3 4207
0479 P01E4 E262
0480                        JPT+  LOWER,NU,NU,NU,NONE,E1,INCTFA,TBRRW      BORROW,DCR-U
0480 P01E5 0061
0480 P01E6 47FE
0480 P01E7 2560
0481                        SEQ   AUEQFF,N1,S2Z,L2,NONE,E1,INCTFA,NU,NU    NO BORROW,DCR DONE
0481 P01E8 E0D0
0481 P01E9 25FF
0482                        SEQ+  AUEQFF,FLE,S1Z,NU,NONE,EB,CLRUDC,LOADFA,$B HERE IF CTR-L=0
0482 P01EA 0062
0482 P01EB E27E
0482 P01EC 30D3
0483                 FLPTUL SEQ   LOWER,NU,NU,NU,NONE,EB,CLRUDC,LOADFA,$B HERE,CTR-L NOT 0
0483 P01ED C7FE
0483 P01EE 30D3
0484                        CMA+  LOWER,L1,OR,BTG,TL1,EN,BG7,NU,NU         LEN-U=0,SET TRM FL
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0484 P01EF 0063
0484 P01F0 808F
0484 P01F1 47FF
0485                    SEQ  UPPER,L1,EOR,BTG,TL1,E2,BG4,LDPCR,$0    FLIP U/L FLAG
0485 P01F2 C8CF
0485 P01F3 54C0
0486                    SEQ+ AUEQFF,L1,ORN,BTG,NONE,EN,BG4,NU,NU     TEST U/L
0486 P01F4 0064
0486 P01F5 E096
0486 P01F6 04FF
0487           CRLFXT JPT  UPPER,FLE,OR,L2,L2F,EN,NU,AQSCAN         FROM CRLFPF AQ WRITE
0487 P01F7 4A09
0487 P01F8 CF0B
0488           FLGTFL SEQ+ LOWER,L1,S1,NU,L2F,EB,LOADFA,PLDUDC,$5   U/L=1,UPPER LAST
0488 P01F9 0065
0488 P01FA C087
0488 P01FB F085
0489                    SEQ  UPPER,L1,AND,CST,TL1,EN,NU,$DE        U/L=0,DAT AV/CRLF OFF
0489 P01FC C8A3
0489 P01FD 4F0E
0490                    JPT+ UPPER,FLE,OR,BTG,L2F,EN,BG1,FLGTFL     T-DMA RQD,FRAB,SEG0
0490 P01FE 0066
0490 P01FF 4A0F
0490 P0200 C165
0491           DOTMT    SEQ  LOWER,NU,NU,NU,NONE,EB,STBCB1,LDPCR,$3  DMA NOT RQD, CS-CD
0491 P0201 C7FE
0491 P0202 3CC3
0492           RCVOFF   SEQ+ UPPER,NU,NU,NU,NONE,E2,NU,RSTPEL,NU     RST PEL/RX OFF
0492 P0203 0067
0492 P0204 CFFE
0492 P0205 1FFF
0493                    SEQ  UPPER,NU,NU,NU,NONE,E2,NU,LDPCR,$B       CS-CD-WR
0493 P0206 CFFE
0493 P0207 1FC8
0494           TROFF3   CMA+ LOWER,N1,S2,CST,TL1,EN,NU,AQSCAN/N-S/N  SET EXIT
0494 P0208 0068
0494 P0209 80A8
0494 P020A 4F08
0495                    SEQ  UPPER,NU,NU,NU,NONE,E2,NU,LDPCR,$0       CONTROLS OFF
0495 P020B CFFE
0495 P020C 1FC0
0496                    XFM+ UPPER,L1,S1,NU,NONE,E1,STBCB1,PRTDDS,NU EXIT,PORT DATA OFF
0496 P020D 0069
0496 P020E 0886
0496 P020F 2C4F
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0498                ECOTMT SEQ  AUEQFF,FLE,ORN,BTG,NONE,EN,BG2,NU,NU      HERE FRA1,SEG1
0498 P0210 E216
0498 P0211 02FF
0499                       SEQ+ UPPER,FLE,ANDN,BTG,L2F,EN,BG2,NU,NU       DATA FOR ECO RDY
0499 P0212 006A
0499 P0213 CA47
0499 P0214 C2FF
0500                       JPT  AUEQFF,FLE,ORN,BTG,NONE,EN,BG3,TROFF1     NO DATA TO ECO
0500 P0215 6216
0500 P0216 036C
0501                       CMA+ LOWER,NU,NU,NU,NONE,E1,INCTFA,NU,NU       FRA OF ECO DATA
0501 P0217 0068
0501 P0218 87FE
0501 P0219 25FF
0502                       JPT  LOWER,FLE,S1,NU,PORTDL,EN,NU,DOTMT        ECO DATA TO TMTR
0502 P021A 4207
0502 P021B 0F66
0503                TROFF1 SEQ+ UPPER,N1,S2,CST,TL1,EN,NU,ECPXOF/N-S/N   HERE TO TERM ECO
0503 P021C 006C
0503 P021D C8AB
0503 P021E 4F73
0504                       JPT  UPPER,NU,NU,NU,NONE,EN,NU,AQSCAN          EXIT
0504 P021F 4FFE
0504 P0220 0F0B
0505                TROFF2 CMA+ LOWER,NU,NU,NU,NONE,E2,NU,LDPCR,$1       CS-CD
0505 P0221 0060
0505 P0222 87FE
0505 P0223 1FC1
0506                       SEQ  UPPER,NU,NU,NU,NONE,E2,NU,LDPCR,$5       CS-CD-RD
0506 P0224 CFFE
0506 P0225 1FC5
0507                       CMA+ LOWER,N1,S2,BTG,TL2,EB,LOADFA,PLDUDC,$9 FA OF LAST URT CMD
0507 P0226 006E
0507 P0227 80AF
0507 P0228 80B9
0508                       SEQ  AUEQFF,PBXI,ORN,BTG,NONE,E2,BG0,LDPCR,$0  TEST TXRDY
0508 P0229 E416
0508 P022A 10C0
0509                       SEQ+ UPPER,FLE,ANDN,L2,PORTDL,EB,STBC81,LDPCR,$1 TXEN OFF IN CMD
0509 P022B 006F
0509 P022C CA41
0509 P022D 3CC1
0510                       JPT  UPPER,NU,NU,NU,NONE,EN,NU,AQSCAN          TXRDY NOT ON
0510 P022E 4FFE
0510 P022F 0F0B
0511                       CMA+ LOWER,FLE,ANDN,L2,L2F,E2,NU,LDPCR,$9      CS-CD-WR,CMD TO FL
0511 P0230 0070
0511 P0231 8241
0511 P0232 0FC9
0512                       SEQ  UPPER,N1,ZERO,NU,L2F,E1,LOADFA,$05        NOP,T FLGS OFF
0512 P0233 C8E7
0512 P0234 E005
0513                       CMA+ LOWER,NU,NU,NU,NONE,E2,NU,LDPCR,$0        CTRLS OFF
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0513 P0235 0071
0513 P0236 87FE
0513 P0237 1FC0
0514                    XFM   UPPER,L1,S1,NU,NONE,E1,STBCB1,PRTODS,NU EXIT
0514 P0238 3886
0514 P0239 2C4F
0515                TRTRM1 CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLOUDC,$E HERE-TX TRM,STWO FRA
0515 P023A 0072
0515 P023B 87FE
0515 P023C 308E
0516                    JPT   UPPER,FLE,OR,BTG,L2F,EN,BG3,TOSTSW      SET T-TRM BIT
0516 P023D 4A0F
0516 P023E C3C4
0517                ECPXOF CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLOUDC,$1 FRA OF R1 FL
0517 P023F 0073
0517 P0240 87FE
0517 P0241 3081
0518                    JPT   UPPER,FLE,ANDN,BTG,L2F,EN,BG3,AQSCAN    CLR ECPLX OFF FLG
0518 P0242 4A47
0518 P0243 C308
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0520                RBCNT   CMA+ LOWER,NU,NU,NU,NONE,E2,NU,CNTUP,NU
0520 P0244 0074
0520 P0245 87FE
0520 P0246 1FEF
0521                TBCNT   SEQ  UPPER,FLE,S1,NU,TL2,E1,INCTFA,NU,NU      CTR-L TO L2
0521 P0247 CA07
0521 P0248 A5FF
0522                        CMA+ LOWER,FLE,S1,NU,TL1,E1,INCTFA,NU,NU      CTR-U TO L1
0522 P0249 0075
0522 P024A 8207
0522 P024B 65FF
0523                        SEQ  UPPER,NU,NU,NU,NONE,E1,INCTFA,NU,NU
0523 P024C CFFE
0523 P024D 25FF
0524                        SEQ+ CYNOT,FLE,MINUS,L2,ATL,EB,ARITHC,CNTDWN,NU
0524 P024E 0076
0524 P024F F248
0524 P0250 830F
0525                UBCSUB  JPT  LOWER,FLE,MINUS,L2,ATU,E1,ARITHC,RPLAQS
0525 P0251 4248
0525 P0252 6387
0526                        JPT+ LOWER,L1,PLUS1,NU,TL2,E1,ARITHC,UBCSUB   BORROW
0526 P0253 0077
0526 P0254 40FF
0526 P0255 A376
0527                        JPT  LOWER,L1,S1,NU,TL2,EN,NU,UBCSUB          NO BORROW
0527 P0256 4087
0527 P0257 8F76
0528                EXTSWR  CMA+ LOWER,NU,NU,NU,NONE,E1,LOADFA,$0D        FRA D,SEG1
0528 P0258 0078
0528 P0259 87FE
0528 P025A 200D
0529                        JPT  LOWER,FLE,S1,NU,ATL,E1,RPLYAQ,ZTXSW      EX STW TO AL
0529 P025B 4206
0529 P025C AA84
0530                SUBFUN  CMA+ LOWER,NAL,NS1AND,CST,TL2,E1,CLRUDC,$07   3 LSBS TO L2
0530 P025D 0079
0530 P025E 8368
0530 P025F AD07
0531                        SEQ  AUEQFF,L1,OR,CST,NONE,E1,SFTL2R,$0F      TST FOR EOT
0531 P0260 E08A
0531 P0261 260F
0532                        SEQ+ UPPER,L1,ANDN,CST,L2F,E1,LOADFA,$F0        *****HERE IF EOT
0532 P0262 007A
0532 P0263 C8C3
0532 P0264 E0F0
0533                        JPT  AUX1,N1,S2,L2,TL1,EN,L2BIT7,SFXFM        HERE NOT EOT
0533 P0265 50A9
0533 P0266 477C
0534                        CMA+ LOWER,FAD,OR,L2,FA,EN,NU,NU,NU           FA TO EOT LOC
0534 P0267 007B
0534 P0268 8388
0534 P0269 CFFF
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0535                        JPT   UPPER,NAU,S1Z,NU,L2F,E1,RPLYAQ,AQSCAN   EOT TO FILE
0535 P026A 4AFF
0535 P026B EA03
0536                  SFXFM SEQ+  UPPER,NAU,S1Z,NU,TL2,E1,RPLYAQ,NU,NU    HERE-DOUBLE,AU TO L2
0536 P026C 007C
0536 P026D CAFF
0536 P026E AAFF
0537                        XFM   UPPER,L1,PLUS,CST,NONE,E1,ARITHN,SFJT/N-S/N  HERE IF SINGLE
0537 P026F 0882
0537 P0270 227E
0538                        CMA+  LOWER,L1,ANDN,BTG,TL1,EN,BG7,NU,NU          STRIP MSB
0538 P0271 007D
0538 P0272 80C7
0538 P0273 47FF
0539                        XFM   LOWER,L1,PLUS,CST,NONE,E1,ARITHN,SFJT/N-S/N  DOUBLE
0539 P0274 0082
0539 P0275 227E
0540                  SFJT  JPT+  UPPER,NU,NU,NU,NONE,E1,RPLYAQ,CRLFPF    CR-LF PFX
0540 P0276 007E
0540 P0277 4FFE
0540 P0278 2A82
0541                        JPT   LOWER,N1,S2Z,BTG,TL1,EN,BG6,PRTCMD      PORT CMD
0541 P0279 4007
0541 P027A 4689
0542                        JPT+  UPPER,NU,NU,NU,NONE,E1,RPLYAQ,INSTLF    INSERT LF
0542 P027B 007F
0542 P027C 4FFE
0542 P027D 2A85
0543                        JPT   UPPER,NU,NU,NU,NONE,EN,NU,RFWAH         R FWA-H
0543 P027E 4FFE
0543 P027F 0F80
0544                        JPT+  UPPER,NU,NU,NU,NONE,E1,RPLYAQ,ECPLOF    ECO PLX OFF
0544 P0280 0080
0544 P0281 4FFE
0544 P0282 2A86
0545                        JPT   UPPER,NU,NU,NU,NONE,EN,NU,TFWAH         T FWA-H
0545 P0283 4FFE
0545 P0284 0F8E
0546                        JPT+  UPPER,NU,NU,NU,NONE,E1,RPLYAQ,ECPLON    ECO PLX ON
0546 P0285 0081
0546 P0286 4FFE
0546 P0287 2A88
0547                        JPT   UPPER,NU,NU,NU,NONE,EN,NU,MFWAH         M FWA-H
0547 P0288 4FFE
0547 P0289 0F8F
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0549                    CRLFPF CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,CNTDWN,$4  T-DATA-L,FRA4,SEG3
0549 P028A 0082
0549 P028B 87FE
0549 P028C 30D4
0550                           SEQ  UPPER,N1,S2,CST,L2F,EN,NU,$0A            LINE FEED
0550 P028D C8AB
0550 P028E CF0A
0551                           CMA+ LOWER,N1,S2,CST,L2F,E1,INCTFA,$0D        CR TO FILE
0551 P028F 0083
0551 P0290 80AB
0551 P0291 E50D
0552                           SEQ  UPPER,N1,S2,BTG,TL1,E2,BG5,PLDUDC,$1     SEG1,FRA 5/CRLF FLG
0552 P0292 C8AF
0552 P0293 5581
0553                           JPT+ LOWER,L1,OR,BTG,TL2,EN,BG0,CRLFXT        T-DATA AV FLG
0553 P0294 0084
0553 P0295 408F
0553 P0296 8064
0554                    ZTXSW  JPT  UPPER,N1,ZERO,NU,L2F,EN,NU,AQSCAN        HERE FROM EXTSWR
0554 P0297 48E7
0554 P0298 CF08
0555                    INSTLF CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$5 FRA5,SEG1
0555 P0299 0085
0555 P029A 87FE
0555 P029B 3085
0556                           JPT  UPPER,FLE,OR,BTG,L2F,EN,BG1,AQSCAN       INST LFT-FLAG
0556 P029C 4A0F
0556 P029D C10B
0557                    ECPLOF CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$1 FRA1,SEG1
0557 P029E 0086
0557 P029F 87FE
0557 P02A0 3081
0558                           SEQ  UPPER,FLE,AND,CST,TL1,EN,NU,$FC          CLR ECO FLAGS
0558 P02A1 CA23
0558 P02A2 4FFC
0559                           JPT+ UPPER,L1,OR,BTG,L2F,EN,BG3,AQSCAN        TERM FLAG ON
0559 P02A3 0087
0559 P02A4 488F
0559 P02A5 C308
0560                    RPLAQS JPT  UPPER,NU,NU,NU,NONE,E1,RPLYAQ,AQSCAN     COMMON RETURN/RPLY
0560 P02A6 4FFE
0560 P02A7 2A0B
0561                    ECPLON CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$1 FRA1,SEG1
0561 P02A8 0088
0561 P02A9 87FE
0561 P02AA 3081
0562                           SEQ  UPPER,FLE,OR,CST,L2F,EN,NU,$03           ECO FLAGS ON
0562 P02AB CA0B
0562 P02AC CF03
0563                           CMA+ LOWER,N1,S2,CST,TL2,EN,NU,$23            RTS,DTR,TXEN ON
0563 P02AD 0089
0563 P02AE 80AB
0563 P02AF 8F23
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0564                PRTCMD SEQ  UPPER,L1,AND,L2,TL2,EB,LOADFA,PLDUDC,$9  LAST URT CMD
0564 P02B0 C8A1
0564 P02B1 B089
0565                       CMA+ LOWER,FLE,AND,CST,TL1,EN,NU,$15          GET LAST
0565 P02B2 008A
0565 P02B3 8223
0565 P02B4 4F15
0566                CMDSEQ SEQ  UPPER,L1,OR,L2,PORTDL,EB,STBCB1,LDPCR,$1  CS-CD-DATA
0566 P02B5 C889
0566 P02B6 3CC1
0567                       CMA+ LOWER,L1,OR,L2,TL1,E2,NU,LDPCR,$9        CS-CD-WR
0567 P02B7 0088
0567 P02B8 8089
0567 P02B9 5FC9
0568                       SEQ  UPPER,L1,AND,CST,L2F,EN,NU,$EF           MASK OUT ER BIT
0568 P02BA C8A3
0568 P02BB CFEF
0569                       CMA+ LOWER,NU,NU,NU,NONE,E2,NU,LDPCR,$0        CTRLS OFF
0569 P02BC 008C
0569 P02BD 87FE
0569 P02BE 1FC0
0570                       SEQ  LOWER,N1,ONES,NU,FA,E1,STBCB1,PRTODS,NU FORCE FA TO NU LOC
0570 P02BF C09E
0570 P02C0 EC4F
0571                RFWAH  CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$2   FRA2,SEG2
0571 P02C1 008D
0571 P02C2 87FE
0571 P02C3 3082
0572                       JPT  UPPER,N1,S2,L2,L2F,EN,NU,AQSCAN
0572 P02C4 48A9
0572 P02C5 CF0B
0573                TFWAH  CMA+ LOWER,N1,S2,L2,L2F,EB,LOADFA,PLDUDC,$6    FRA6,SEG2
0573 P02C6 008E
0573 P02C7 80A9
0573 P02C8 F0B6
0574                       SEQ  LOWER,NU,NU,NU,NONE,E1,LOADFA,$0C         FRA-C,SEG2
0574 P02C9 C7FE
0574 P02CA 200C
0575                MFWAH  CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$A   FRAA,SEG2
0575 P02CB 008F
0575 P02CC 87FE
0575 P02CD 3088
0576                       JPT  UPPER,N1,S2,L2,L2F,EN,NU,AQSCAN
0576 P02CE 48A9
0576 P02CF CF0B
0577                RLEN   SEQ+ AUEQFF,NAU,S1,NU,TL2,EB,RPLYAQ,LOADFA,$5  HERE IF AL=00
0577 P02D0 0090
0577 P02D1 E287
0577 P02D2 8A05
0578                       SEQ  LOWER,NAU,S1,NU,TL2,E1,RPLYAQ,NU,NU       HERE AL NOT 00,SEG1
0578 P02D3 C287
0578 P02D4 4AFF
0579                       JPT+ UPPER,N1,S2,BTG,TL2,EN,BG2,RLZTRM         HERE IF LEN=00
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0579 P02D5 0091
0579 P02D6 48AF
0579 P02D7 824E
0580                    SEQ  UPPER,N1,S2Z,L2,L2F,E1,LOADFA,$03        STOR AU
0580 P02D8 C8D1
0580 P02D9 E003
0581                    CMA+ LOWER,L1,S1Z,NU,L2F,EB,LOADFA,CNTUP,$3  STOR AL
0581 P02DA 0092
0581 P02DB 80FF
0581 P02DC F0E3
0582                    SEQ  UPPER,N1,S2,L2,L2F,E1,LOADFA,$00        LEN-L TO CTR-L
0582 P02DD C8A9
0582 P02DE E000
0583                    CMA+ LOWER,N1,ZERO,NU,L2F,E2,NU,CNTDWN,NU    ZERO TO U/L FLAG
0583 P02DF 0093
0583 P02E0 80E7
0583 P02E1 0F0F
0584                    SEQ  UPPER,NU,NU,NU,NONE,E1,LOADFA,$01       FRA1,SEG1-R1 FL
0584 P02E2 CFFE
0584 P02E3 2091
0585                    CMA+ LOWER,FLE,OR,BTG,L2F,EN,BG5,NU,NU       RBA FLAG ON
0585 P02E4 0094
0585 P02E5 820F
0585 P02E6 C5FF
0586                    SEQ  UPPER,NU,NU,NU,NONE,E1,LOADFA,$03       FA OF LEN-U,SEG1
0586 P02E7 CFFE
0586 P02E8 2003
0587                    CMA+ LOWER,FLE,S1,NU,L2F,EB,LOADFA,CNTUP,$1  FA OF CTR-U
0587 P02E9 0095
0587 P02EA 8207
0587 P02EB F0E1
0588                    SEQ  UPPER,N1,S2,BTG,TL2,E2,BG4,PLDUDC,$1    ER BIT FOR RXEN
0588 P02EC C8AF
0588 P02ED 9481
0589                    CMA+ LOWER,FLE,S1,NU,TL1,EB,LOADFA,PLDUDC,$9 LAST URT CMD FA
0589 P02EE 0096
0589 P02EF 8207
0589 P02F0 7089
0590                    SEQ  AUEQFF,L1,OR,CST,NONE,EN,NU,$FC         TEST FOR ECO PLX
0590 P02F1 E08A
0590 P02F2 0FFC
0591                    CMA+ LOWER,FLE,OR,CST,TL2,EN,NU,$31          ECO PLX-RTS,TXEN ON
0591 P02F3 0097
0591 P02F4 8208
0591 P02F5 8F31
0592                    JPT  LOWER,FLE,OR,BTG,TL1,EN,BG2,CMDSEQ      NOT ECO PLX-RXEN ON
0592 P02F6 420F
0592 P02F7 428A
0593            RFWA16  CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$2 FRA2,SEG2-FWAH
0593 P02F8 0098
0593 P02F9 87FE
0593 P02FA 3082
0594            FWASEQ  SEQ  UPPER,N1,ZERO,NU,L2F,EN,NU,NU,NU        ZERO FWA-H
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0594 P02FB C8E7
0594 P02FC CFFF
0595                    CMA+ LOWER,NAL,S1Z,NU,L2F,EB,RPLYAQ,CNTUP,NU FWA-L
0595 P02FD 0099
0595 P02FE 837F
0595 P02FF FAEF
0596                    JPT  UPPER,L1,S1,NU,L2F,E1,INCTFA,AQSCAN      FWA-U
0596 P0300 4887
0596 P0301 E50B
0597                MFWA16 CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$5 FRA5,SEG1-FLG T1
0597 P0302 009A
0597 P0303 87FE
0597 P0304 3085
0598                    SEQ  UPPER,FLE,OR,BTG,L2F,EN,BG3,NU,NU        SET DNAY FLAG
0598 P0305 CA0F
0598 P0306 C3FF
0599                    CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$A FRA-A,SEG2-FWAH
0599 P0307 009B
0599 P0308 87FE
0599 P0309 30BA
0600                    JPT  LOWER,NU,NU,NU,NONE,EN,NU,FWASEQ         FINISH ABOVE
0600 P030A 47FE
0600 P030B 0F98
0601                TFWA16 CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$6 FRA6,SEG2-FWAH
0601 P030C 009C
0601 P030D 87FE
0601 P030E 30B6
0602                    SEQ  UPPER,N1,ZERO,NU,L2F,EN,NU,NU,NU         ZERO T-FWA-H
0602 P030F C8E7
0602 P0310 CFFF
0603                    CMA+ LOWER,NAU,S1Z,NU,L2F,EB,LOADFA,CNTUP,$7 T-FWA-U
0603 P0311 009D
0603 P0312 82FF
0603 P0313 F0E7
0604                    SEQ  UPPER,NAL,S1Z,NU,L2F,EB,RPLYAQ,LOADFA,$6  T-FWA-L
0604 P0314 C87F
0604 P0315 FA06
0605                    CMA+ LOWER,N1,S2,L2,L2F,E1,LOADFA,$C           MD-FWA-L
0605 P0316 009E
0605 P0317 80A9
0605 P0318 E00C
0606                    JPT  UPPER,L1,S1,NU,L2F,E1,INCTFA,AQSCAN       MD-FWA-H
0606 P0319 4887
0606 P031A E50B
0607                TSTTLU JPT+ LOWER,FAD,PLUS,ETG,FA,E1,ARITHN,TLENZ  HERE,BOTH=0,TO FRA5
0607 P031B 009F
0607 P031C 4386
0607 P031D E281
0608                    SEQ  LOWER,NU,NU,NU,NONE,EN,NU,NU,NU          HERE,AL=0,AU NOT
0608 P031E C7FE
0608 P031F 0FFF
0609                TLEN   JPT+ AUEQFF,NAU,S1,NU,TL2,E1,INCTFA,TSTTLU  HERE,AL=0
0609 P0320 00A0
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0609 P0321 6237
0609 P0322 A59F
0610                    SEQ  UPPER,NAL,S1Z,NU,L2F,EB,LOADFA,CNTUP,$4 HERE,LEN NOT=0
0610 P0323 C87F
0610 P0324 F0E4
0611                    CMA+ LOWER,NAU,S1Z,NU,L2F,EB,RPLYAQ,LOADFA,$5 STOR CTR-U
0611 P0325 00A1
0611 P0326 82FF
0611 P0327 FA05
0612                    SEQ  UPPER,N1,S2,L2,L2F,EB,LOADFA,CNTDWN,$7   STOR LEN-U,SEG1
0612 P0328 C8A9
0612 P0329 F007
0613                    CMA+ LOWER,L1,S1Z,NU,L2F,E2,NU,PLDUDC,$2      STOR LEN-L,SEG2
0613 P032A 00A2
0613 P032B 80FF
0613 P032C DF82
0614                    SEQ  UPPER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$5  FLAG T1,FRA5,SEG1
0614 P032D CFFE
0614 P032E 3085
0615                    CMA+ LOWER,FLE,ANDN,BTG,L2F,EN,BG4,NU,NU      TX U/L FL TO 0
0615 P032F 00A3
0615 P0330 8247
0615 P0331 C4FF
0616                    SEQ  AUX1,NU,NU,NU,NONE,E2,L2BIT0,LOADFA,$B  TEST B.DATA AVAIL
0616 P0332 07FE
0616 P0333 1609
0617               TXENBT SEQ+ UPPER,N1,S2,BTG,TL2,EB,BG0,PLDUDC,$9   DATA AV.FLG ON
0617 P0334 00A4
0617 P0335 C8AF
0617 P0336 8089
0618                    JPT  LOWER,NU,NU,NU,NONE,E1,CLRUDC,TLDMAR    SET SEG0
0618 P0337 47FE
0618 P0338 20A7
0619                    CMA+ LOWER,FLE,OR,L2,PORTDL,EB,STBCB1,LDPCR,$1 TXEN TO LAST URTC
0619 P0339 00A5
0619 P033A 8209
0619 P033B 3CC1
0620                    SEQ  UPPER,FLE,OR,L2,L2F,E2,NU,LDPCR,$9       CS-CD-WR
0620 P033C CA09
0620 P033D DFC9
0621                    CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$5  TO FLAG T1
0621 P033E 00A6
0621 P033F 87FE
0621 P0340 3085
0622                    SEQ  UPPER,N1,S2,BTG,TL2,E2,BG3,LDPCR,$0      CTRLS OFF
0622 P0341 C8AF
0622 P0342 93C0
0623                    SEQ+ AUEQFF,FLE,ORN,L2,NONE,E1,STBCB1,PRTDOS,NU  TEST DNAY IN T1
0623 P0343 00A7
0623 P0344 E210
0623 P0345 2C4F
0624               TLDMAR JPT  UPPER,FLE,OR,BTG,L2F,EN,BG1,TXENBT     NOT ON,SET DMA RQD
0624 P0346 4A0F
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0624 P0347 C1A4
0625                    SEQ+ UPPER,NU,NU,NU,NONE,EB,LOADFA,CNTUP,$4  ONAY FLG ON,TO SEG2
0625 P0348 00A8
0625 P0349 CFFE
0625 P034A 30E4
0626                    JPT  UPPER,NU,NU,NU,NONE,EN,NU,ECPXOF        FLG NOT ON,DONE
0626 P034B 4FFE
0626 P034C 0F73
0627                    CMA+ LOWER,FLE,S1,NU,TL1,E1,LOADFA,$05       GET CTR-L,FA TO U
0627 P034D 00A9
0627 P034E 8207
0627 P034F 6005
0628                    SEQ  UPPER,FLE,S1,NU,L2F,E1,LOADFA,$09     T-CTR-U TO M-CTR-U
0628 P0350 CA07
0628 P0351 E009
0629            RNDUPL JPT+ CYNOT,L1,PLUS1,NU,TL1,E1,ARITHC,RNDUPU  T-CTR-L PLUS 1
0629 P0352 00AA
0629 P0353 70FF
0629 P0354 63AE
0630            CLONAY JPT  UPPER,FLE,ANDN,BTG,L2F,EN,BG3,RQBMVF    **FROM/TO LMCMS RTN*
0630 P0355 4A47
0630 P0356 C3E1
0631            MLEN   JPT+ AUEQFF,NAU,S1,NU,TL1,EN,NU,MLENA        HERE IF AL=0
0631 P0357 00AB
0631 P0358 6287
0631 P0359 4FAC
0632                    SEQ  LOWER,NU,NU,NU,NONE,EN,NU,NU,NU        AL NOT=0
0632 P035A C7FE
0632 P035B 3FFF
0633            MLENA  JPT+ UPPER,NU,NU,NU,NONE,E1,RJCTAQ,AGSCAN    HERE IF AU=0 (BOTH)
0633 P035C 00AC
0633 P035D 4FFE
0633 P035E 2B08
0634                    SEQ  UPPER,NAU,S1Z,NU,L2F,EB,LOADFA,CNTUP,$9 AU NOT=0,STOR AU
0634 P035F CAFF
0634 P0360 F0E9
0635                    JPT+ UPPER,NAL,S1Z,NU,TL1,E1,RPLYAQ,RNDUPL   M-CTR-L TO L1
0635 P0361 00AD
0635 P0362 487F
0635 P0363 6AAA
0636            MOETST JPT  AUEQFF,FLE,ORN,BTG,NONE,EN,BG0,OESTAT   **FROM RXRDY RTN**
0636 P0364 6216
0636 P0365 0080
0637            RNDUPU SEQ+ UPPER,L1,ANDN,BTG,L2F,E2,BG0,LOADFA,$8  NO CARRY,STRIP LSB
0637 P0366 00AE
0637 P0367 C8C7
0637 P0368 0008
0638                    CMA  UPPER,FLE,PLUS1,NU,L2F,E1,ARITHC,NU,NU  HERE-CARRY (FRA=9)
0638 P0369 8A7F
0638 P036A E3FF
0639                    CMA+ LOWER,NU,NU,NU,NONE,EB,CLRUDC,LOADFA,$B TO R2 FLAGS
0639 P036B 00AF
0639 P036C 87FE
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0639 P036D 3D0B
0640                    JPT   UPPER,FLE,OR,BTG,L2F,EN,BG3,ECPXOF      RQST PRIORITY BLK MV
0640 P036E 4A0F
0640 P036F C373
0641                OESTAT CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,CNTDWN,$E MEM OVRN ER TO ST WD
0641 P0370 00B0
0641 P0371 87FE
0641 P0372 3D0E
0642                    JPT   UPPER,FLE,OR,BTG,L2F,EN,BG4,RDURT       **RET TO RXRDY RTN**
0642 P0373 4A0F
0642 P0374 C439
0643                    FIL+
0643 P0375 00B1
0643 P0376 8800
     P0377 0000
0644                TLENZ  SEQ   UPPER,FLE,OR,CST,L2F,E1,RPLYAQ,$80     SET T-TRM BIT
0644 P0378 CA0B
0644 P0379 EA80
0645                    CMA+ LOWER,NU,NU,NU,NONE,EB,CLRUDC,LOADFA,$B TO FLAG R2
0645 P037A 00B2
0645 P037B 87FE
0645 P037C 3D0B
0646                    JPT   UPPER,FLE,ANDN,BTG,L2F,EN,BG1,TLZX      CLR T DMA RQ
0646 P037D 4A47
0646 P037E C156
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0648                 DMAFL1 SEQ+ UPPER,N1,S2,CST,FA,E1,CLRUDC,$1C        HERE-DMA AVAILABLE
0648 P037F 00B3
0648 P0380 C8AA
0648 P0381 ED1C
0649                        JPT  UPPER,NU,NU,NU,NONE,EN,NU,TXRDY1        GO TO TXRDY RTN
0649 P0382 4FFE
0649 P0383 0F54
0650                        SEQ+ AUEQFF,FLE,S1Z,NU,TL1,EN,NU,NU,NU       GET LMCXX/(IN L1)
0650 P0384 00B4
0650 P0385 E27F
0650 P0386 4FFF
0651                 DPRTFA JPT  UPPER,L1,S1Z,NU,TL2,E1,INCFPA,GETPRT     FA TO 2C, PORT
0651 P0387 48FF
0651 P0388 A488
0652                 NXTRQS SEQ+ UPPER,N1,S2,CST,FA,E1,CLRUDC,$3C         LMCXX=00,DO NEXTRQS
0652 P0389 00B5
0652 P038A C8AA
0652 P038B ED3C
0653                        JPT  LOWER,N1,ZERO,NU,L2F,EN,NU,DPRTFA       LMC SET, CLR TO 00
0653 P038C 40E7
0653 P038D CFB4
0654                        CMA+ LOWER,FLE,PLUS,CST,L2F,E1,ARITHN,$10    INCR LAST-RESTORE
0654 P038E 00B6
0654 P038F 8233
0654 P0390 E210
0655                        SEQ  UPPER,N1,S2,CST,TL2,EN,NU,$0C           BMV CLR FLG BITS
0655 P0391 C8AB
0655 P0392 9F0C
0656                        CMA+ LOWER,FLE,OR,CST,FA,E1,LDPNR,$0B        TO FA OF FLAG R2
0656 P0393 00B7
0656 P0394 821A
0656 P0395 EF0B
0657                        SEQ  AUEQFF,FLE,NAND,CST,NONE,EN,NU,$0F      IS ANY DMA RQD
0657 P0396 E25A
0657 P0397 0F0F
0658                        JPT+ UPPER,NU,NU,NU,NONE,EN,NU,TXRDY1        HERE-NO DMA RQD
0658 P0398 00B8
0658 P0399 4FFE
0658 P039A 0F54
0659                        SEQ  AUEQFF,FLE,NAND,CST,NONE,EN,NU,$03      IS IT A PORT
0659 P039B E25A
0659 P039C 0F03
0660                 DOBMVF JPT+ LOWER,FLE,ANDN,L2,L2F,EN,NU,MFDMA        NOT A PORT-BMV-F
0660 P039D 00B9
0660 P039E 4241
0660 P039F CFEB
0661                        SEQ  AUEQFF,FLE,ORN,BTG,NONE,EN,BGO,NU,NU    A PORT NEEDS DMA
0661 P03A0 E216
0661 P03A1 00FF
0662                        JPT+ UPPER,FLE,ANDN,BTG,L2F,EN,BGO,RSDMA     RCVR HAS DATA
0662 P03A2 00BA
0662 P03A3 4A47
0662 P03A4 C0E2
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0663                        JPT   AUEQFF,FLE,ORN,BTG,NONE,EN,BG3,TFDMA    TMTR NEEDS DATA
0663 P03A5 6216
0663 P03A6 03E7
0664                  GETPRT CMA+ LOWER,FLE,AND,CST,TL1,EN,NU,$F0          PPPP0000 TO L1
0664 P03A7 00BB
0664 P03A8 8223
0664 P03A9 4FF0
0665                        XFM   AUX1,N1,S2,L2,NONE,E2,NOTERR,PLDUDC,$1  GOES LOWER IF MEMERR
0665 P03AA 10A8
0665 P03AB 10B1
0666                  LMCTF  SEQ+ UPPER,L1,OR,BTG,FA,E2,BG2,PLDUDC,$3      TO TX DATA-L
0666 P03AC 00BC
0666 P03AD C88E
0666 P03AE D283
0667                        JPT   LOWER,L1,S1,NU,FA,E1,LDPNR,TFME          HERE IF ME
0667 P03AF 4086
0667 P03B0 EF8E
0668                        JPT+  LOWER,DFL,S1,NU,L2F,EN,NU,STORUP         STOR TX DATA-L
0668 P03B1 00BD
0668 P03B2 4107
0668 P03B3 CF0C
0669                  LMCTFX SEQ  UPPER,NU,NU,NU,NONE,E2,NU,PLDUDC,$1      TO FRA5,SEG1-FL T1
0669 P03B4 CFFE
0669 P03B5 1FB1
0670                        JPT+  UPPER,FLE,OR,BTG,L2F,EN,BG0,NXTRQS      SET TX DATA AV FLG
0670 P03B6 00BE
0670 P03B7 4A0F
0670 P03B8 C0B5
0671                  TFME   SEQ  AUX1,NU,NU,NU,NONE,E2,MAE,LOADFA,$D      TO EX ST WD
0671 P03B9 D7FE
0671 P03BA 1F0D
0672                        SEQ+  UPPER,FLE,OR,CST,L2F,E1,CLRERR,$80       HERE MAE
0672 P03BB 003F
0672 P03BC CA0B
0672 P03BD E180
0673                        SEQ   UPPER,FLE,OR,CST,L2F,E1,CLRERR,$08       HERE MPE
0673 P03BE CA0B
0673 P03BF E108
0674                        CMA+  LOWER,NU,NU,NU,NONE,EB,INCTFA,PLDUDC,$3  TO SEG 3
0674 P03C0 00C0
0674 P03C1 87FE
0674 P03C2 3533
0675                        JPT   UPPER,FLE,OR,BTG,L2F,EN,BG0,LMCTF        EXT BIT ON
0675 P03C3 4A0F
0675 P03C4 C0BC
0676                  LMCRS  SEQ+ UPPER,L1,OR,CST,FA,E1,CLRUDC,$0B         TO FLAG R2 (NO ME)
0676 P03C5 00C1
0676 P03C6 C88A
0676 P03C7 ED0B
0677                        SEQ   LOWER,L1,OR,CST,FA,E1,LDPNR,$0D          HERE IF ME-EXT STWD
0677 P03C8 C08A
0677 P03C9 EF0D
0678                        SEQ+  AUEQFF,FLE,ORN,BTG,NONE,EN,BG7,NU,NU     TST FOR RCVR TERM
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0678 P03CA 00C2
0678 P03CB E216
0678 P03CC 07FF
0679                    JPT   AUX1,NU,NU,NU,NONE,EN,MAE,RSME          GO SET ERROR BITS
0679 P03CD 57FE
0679 P03CE 3FC5
0680          RCVEND    SEQ+  UPPER,FLE,ANDN,CST,L2F,E2,NU,RSTPEL,$1  CLR R FLAGS
0680 P03CF 00C3
0680 P03D0 CA43
0680 P03D1 0FF1
0681                    JPT   UPPER,NU,NU,NU,NONE,EN,NU,NXTRQS        TERM NOT ON-NEXT RQ
0681 P03D2 4FFE
0681 P03D3 3F35
0682          TOSTSW    CMA+  LOWER,FAD,OR,CST,FA,EN,NU,$0F           SET FA FOR STKSTW
0682 P03D4 00C4
0682 P03D5 838A
0682 P03D6 CF3F
0683                    JPT   UPPER,FAD,MINUS1,NU,FA,E1,ARITHN,STKSTW SET FRA-E
0683 P03D7 4886
0683 P03D8 E21D
0684          RSME      SEQ+  UPPER,FLE,OR,CST,L2F,E1,CLRERR,$40      HERE MAE
0684 P03D9 00C5
0684 P03DA CA0B
0684 P03DB E140
0685                    SEQ   UPPER,FLE,OR,CST,L2F,E1,CLRERR,$04      HERE MPE
0685 P03DC CA0B
0685 P03DD E104
0686                    CMA+  LOWER,NU,NU,NU,NONE,EB,INCTFA,PLDUDC,$3 TO ST WD
0686 P03DE 00C6
0686 P03DF 87FE
0686 P03E0 3583
0687                    JPT   UPPER,FLE,OR,BTG,L2F,EN,BG0,LMCRS       SET EXT BIT,CONTINUE
0687 P03E1 4A0F
0687 P03E2 C0C1
0688          MFME      SEQ+  UPPER,FLE,OR,CST,L2F,E1,CLRERR,$20      HERE MAE
0688 P03E3 00C7
0688 P03E4 CA0B
0688 P03E5 E120
0689                    SEQ   UPPER,FLE,OR,CST,L2F,E1,CLRERR,$02      HERE MPE
0689 P03E6 CA0B
0689 P03E7 E102
0690                    CMA+  LOWER,NU,NU,NU,NONE,EB,INCTFA,PLDUDC,$3 FA TO ST WD
0690 P03E8 00C8
0690 P03E9 87FE
0690 P03EA 3583
0691                    SEQ   UPPER,FLE,OR,CST,L2F,EN,NU,$01          SET EXT BIT
0691 P03EB CA0B
0691 P03EC CF01
0692          LMCMF     SEQ+  LOWER,N1,S2,CST,FA,E1,CLRUDC,$1C        LMC LOC FOR MSDMA
0692 P03ED 00C9
0692 P03EE C0AA
0692 P03EF ED1C
0693                    SEQ   UPPER,L1,OR,CST,FA,E1,LDPNR,$0D         HERE-MEM ERR,SEG1
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0693 P03F0 C88A
0693 P03F1 EF0D
0694                    JPT+ AUX1,NU,NU,NU,NONE,EN,MAE,MFME          FRA OF EXT ST WD
0694 P03F2 00CA
0694 P03F3 57FE
0694 P03F4 0FC7
0695                    SEQ  UPPER,NU,NU,NU,NONE,EN,NU,NU,NU         NOP
0695 P03F5 CFFE
0695 P03F6 1FFF
0696                    CMA+ LOWER,OFL,S1,NU,TL2,E2,NU,LODTL,NU      LOWER MOVE DATA
0696 P03F7 00CB
0696 P03F8 8107
0696 P03F9 9F2F
0697                    SEQ  UPPER,OFU,S1,NU,TL2,E2,NU,LODTU,NU      UPPER MOVE DATA
0697 P03FA C987
0697 P03FB 9F3F
0698             MSDMA  CMA+ LOWER,N1,S2,CST,L2F,EN,NU,LMCMS/N-S/N   SET LMC
0698 P03FC 00CC
0698 P03FD 80AB
0698 P03FE CFD0
0699                    SEQ  UPPER,L1,S1,NU,FA,EB,LDPNR,PLDUDC,$2    SET FPA/SEG MV-CTR-L
0699 P03FF C886
0699 P0400 FF82
0700                    CMA+ LOWER,NU,NU,NU,NONE,EB,STBCB1,CLRRD,$8  CLRRD=LOADFA=0
0700 P0401 00CD
0700 P0402 87FE
0700 P0403 3C08
0701                    SEQ  CYNOT,FLE,MINUS,CST,L2F,E1,ARITHC,$02   DCR MV CTR BY 2 BYTS
0701 P0404 F24B
0701 P0405 E302
0702                    JPT+ UPPER,NU,NU,NU,NONE,E1,INCTFA,MSBRRW    BORROW-NOT ZERO
0702 P0406 00CE
0702 P0407 4FFE
0702 P0408 2501
0703                    SEQ  AUEQFF,N1,S2Z,L2,NONE,E1,INCTFA,NU,NU   NO BORROW-CK L FOR 0
0703 P0409 E000
0703 P040A 25FF
0704                    SEQ+ AUEQFF,FLE,S1Z,NU,NONE,EB,LOADFA,PLDUDC,$5   CTR-L=0,CK UPPR
0704 P040B 00CF
0704 P040C E27E
0704 P040D 3085
0705                    SEQ  LOWER,NU,NU,NU,NONE,EN,NU,NU,NU         HERE-L NOT ZERO-DONE
0705 P040E C7FE
0705 P040F 1FFF
0706                    CMA+ LOWER,FLE,OR,BTG,L2F,EN,BG2,NU,NU       HERE-BOTH ZERO-TERM
0706 P0410 00D0
0706 P0411 820F
0706 P0412 C2FF
0707                    SEQ  LOWER,NU,NU,NU,NONE,E2,NU,PLDUDC,$2     HERE-UPPR NOT ZERO
0707 P0413 C7FE
0707 P0414 1F82
0708             MSBRRW CMA+ LOWER,FLE,MINUS1,NU,L2F,E1,ARITHN,NU,NU DECR UPPER,SEG2
0708 P0415 00D1
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0708 P0416 8207
0708 P0417 E2FF
0709                    SEQ  UPPER,NU,NU,NU,NONE,E1,LOADFA,$0C       SET FRA-C FOR MV STR
0709 P0418 CFFE
0709 P0419 200C
0710                DMASEQ CMA+ LOWER,FLE,S1,NU,TL1,E2,NU,LDDMAH,NU     FWA-H TO L1 AND MAD
0710 P041A 0002
0710 P041B 8207
0710 P041C 5F1F
0711                    SEQ  AUEQFF,L1,NAND,CST,NONE,E1,STBCB1,MAB18B,$2  *TEST BIT 18
0711 P041D E00A
0711 P041E 2CD2
0712                    SEQ+ AUEQFF,L1,NAND,BTG,NONE,E2,BG3,PLDUDC,$3 *18=0,TST 20,TO SG3
0712 P041F 0003
0712 P0420 E00E
0712 P0421 1383
0713                    CMA  UPPER,NU,NU,NU,NONE,E1,STBCB1,MAB181,NU  *18=1,OUTPUT TO LO
0713 P0422 8FFE
0713 P0423 2C5F
0714                    SEQ+ UPPER,NU,NU,NU,NONE,E1,STBCB1,MAB200,NU  *20=0,OUTPUT TO HI
0714 P0424 0004
0714 P0425 CFFE
0714 P0426 2C8F
0715                    SEQ  UPPER,NU,NU,NU,NONE,E1,STBCB1,MAB201,NU  *20=1,OUTPUT TO LO
0715 P0427 CFFE
0715 P0428 2C3F
0716                    CMA+ LOWER,FLE,S1,NU,NONE,EB,INCTFA,LDDMAL,NU *DMA ADR-L
0716 P0429 0005
0716 P042A 8206
0716 P042B 356F
0717                    SEQ  UPPER,FLE,S1,NU,NONE,E2,NU,LDDMAU,NU     *DMA ADR-U
0717 P042C CA06
0717 P042D 1F7F
0718                    CMA+ LOWER,FAD,MINUS,CST,FA,E1,ARITHC,$01     FA TO FWA-L
0718 P042E 0006
0718 P042F 83CA
0718 P0430 E301
0719                    SEQ  CYNOT,FLE,PLUS1,NU,L2F,E1,ARITHC,NU,NU  FWA-L PLUS 1
0719 P0431 F27F
0719 P0432 E3FF
0720                    JPT+ UPPER,NU,NU,NU,NONE,E1,CLRDMA,DMAREQ    NO CARRY-DONE
0720 P0433 0007
0720 P0434 4FFE
0720 P0435 2909
0721                    SEQ  UPPER,NU,NU,NU,NONE,EB,CLRDMA,INCTFA,NU CARRY TO FWA-U
0721 P0436 CFFE
0721 P0437 395F
0722                    SEQ+ CYNOT,FLE,PLUS1,NU,L2F,E1,ARITHC,NU,NU  FWA-U PLUS 1
0722 P0438 0008
0722 P0439 F27F
0722 P043A E3FF
0723                FWAHP1 SEQ  UPPER,L1,PLUS1,NU,L2F,EB,ARITHC,CNTDWN,NU FWA-H PLUS 1
0723 P043B C8FF
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0723 P043C F3DF
0724                DMAREQ JPT+ UPPER,NU,NU,NU,NONE,E1,REQDMA,AQSCAN    NO CARRY DONE
0724 P043D 0009
0724 P043E 4FFE
0724 P043F 2808
0725                       JPT  LOWER,FAD,MINUS1,NU,FA,E1,ARITHN,FWAHP1 CARRY TO FWA-H
0725 P0440 4386
0725 P0441 E2D8
0726                MSME   SEQ+ UPPER,FLE,OR,CST,L2F,E1,CLRERR,$10      HERE MAE
0726 P0442 000A
0726 P0443 CA0B
0726 P0444 E110
0727                       SEQ  UPPER,FLE,OR,CST,L2F,E1,CLRERR,$01      HERE MPE
0727 P0445 CA0B
0727 P0446 E101
0728                       CMA+ LOWER,NU,NU,NU,NONE,EB,INCTFA,PLDUDC,$3 FA TO ST WD
0728 P0447 000B
0728 P0448 87FE
0728 P0449 35B3
0729                       SEQ  UPPER,FLE,OR,CST,L2F,EN,NU,$01          SET EXT BIT
0729 P044A CA0B
0729 P044B CF01
0730                       SEQ+ UPPER,NU,NU,NU,NONE,E2,NU,PLDUDC,$1     SET SEG 1
0730 P044C 000C
0730 P044D CFFE
0730 P044E 1FB1
0731                STORUP JPT  LOWER,DFU,S1,NU,L2F,E1,INCTFA,LMCTFX    FROM LMCTF-TX D-U
0731 P044F 4187
0731 P0450 E58D
0732                LMCMS  SEQ+ LOWER,L1,OR,CST,FA,E1,LDPNR,$05         FA OF FLG T1,SEG1
0732 P0451 000D
0732 P0452 C08A
0732 P0453 EF05
0733                       SEQ  UPPER,L1,OR,CST,FA,E1,LDPNR,$0D         HERE-MEM ERR-EX STWD
0733 P0454 C08A
0733 P0455 EF0D
0734                       JPT+ AUX1,NU,NU,NU,NONE,EN,MAE,MSME          TEST MAE/MPE
0734 P0456 000E
0734 P0457 57FE
0734 P0458 3FDA
0735                       SEQ  AUEQFF,FLE,ORN,BTG,NONE,EN,BG2,NU,NU    TEST MV TRM IN FL T1
0735 P0459 E216
0735 P045A 02FF
0736                       SEQ+ UPPER,FLE,ANDN,CST,L2F,EN,NU,$0C        HERE BMV COMPLETE
0736 P045B 000F
0736 P045C CA43
0736 P045D CF0C
0737                       JPT  LOWER,FLE,AND,BTG,TL1,EN,BG3,CLDNAY     HERE-GET DNAY FLAG
0737 P045E 4227
0737 P045F 43AA
0738                       CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$E BMV COMPL-SET STATUS
0738 P0460 00E0
0738 P0461 87FE
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0738 P0462 303E
0739                    JPT   UPPER,FLE,OR,BTG,L2F,EN,BG0,STKSTW      M BIT TO ST WD
0739 P0463 4A0F
0739 P0464 C01D
0740                RQBMVF CMA+ LOWER,L1,ORN,CST,TL2,EB,LOADFA,CNTDWN,$B TO R2 FLGS,L2=$X4
0740 P0465 00E1
0740 P0466 8093
0740 P0467 80CB
0741                    JPT   UPPER,FLE,OR,L2,L2F,EN,NU,NXTRQS        SET BMV-F DMA RQD
0741 P0468 4A09
0741 P0469 CF85
0742                RSDMA  CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,CNTDWN,$0 FRA0,SEG3,R-DATA-L
0742 P046A 00E2
0742 P046B 87FE
0742 P046C 3000
0743                    SEQ   UPPER,FLE,S1,NU,NONE,EB,INCTFA,LDDTL,NU  DATA-L
0743 P046D CA06
0743 P046E 352F
0744                    CMA+ LOWER,FLE,S1,NU,NONE,EB,CLRUDC,LDDTU,NU   DATA-U
0744 P046F 00E3
0744 P0470 8206
0744 P0471 303F
0745                    SEQ   UPPER,FAD,AND,CST,TL1,EN,NU,$F0          SAVE PPPP
0745 P0472 C8A3
0745 P0473 4FF0
0746                    CMA+ LOWER,N1,S2,CST,FA,EN,NU,$1C              FA TO LMC
0746 P0474 00E4
0746 P0475 80AA
0746 P0476 CF1C
0747                    SEQ   UPPER,N1,S2,CST,L2F,EN,NU,LMCRS/N-S/N    SET LMC TO RS
0747 P0477 C8AB
0747 P0478 CFC1
0748                    CMA+ LOWER,L1,S1,NU,L2F,E1,INCFPA,NU,NU        PORT TO FA 2C,SEG0
0748 P0479 00E5
0748 P047A 8087
0748 P047B E4FF
0749                    SEQ   UPPER,NU,NU,NU,NONE,E1,STBCB1,CLRRD,NU   DMA WRITE MODE
0749 P047C CFFE
0749 P047D 2C3F
0750                    CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$2 TO PPPP001C,SEG2
0750 P047E 00E6
0750 P047F 87FE
0750 P0480 3082
0751                    JPT   UPPER,NU,NU,NU,NONE,EN,NU,DMASEQ         DO DMA WRITE
0751 P0481 4FFE
0751 P0482 3FD2
0752                TFDMA  JPT+ UPPER,NU,NU,NU,NONE,EN,NU,DOBMVF       HERE-BMV RQD FIRST
0752 P0483 00E7
0752 P0484 4FFE
0752 P0485 3FB9
0753                    SEQ   UPPER,FLE,ANDN,BTG,L2F,EN,BG1,NU,NU      HERE-DO TMTR FETCH
0753 P0486 CA47
0753 P0487 C1FF
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0754
0754 P0488 00E8
0754 P0489 83A3
0754 P048A 4FF0
0755
0755 P048B C8AA
0755 P048C ED1C
0756
0756 P048D 00E9
0756 P048E 80A8
0756 P048F CFBC
0757
0757 P0490 C887
0757 P0491 E4FF
0758
0758 P0492 00EA
0758 P0493 87FE
0758 P0494 2C8F
0759
0759 P0495 CFFE
0759 P0496 3086
0760
0760 P0497 00EB
0760 P0498 4FFE
0760 P0499 0FD2
0761                MFDMA  SEQ  UPPER,FAD,AND,CST,TL1,EN,NU,$F0          SAVE PPPP0000
0761 P049A CBA3
0761 P049B 4FF0
0762
0762 P049C 00EC
0762 P049D 80AA
0762 P049E ED1C
0763
0763 P049F C8AB
0763 P04A0 CFC9
0764
0764 P04A1 00ED
0764 P04A2 8087
0764 P04A3 E4FF
0765
0765 P04A4 CFFE
0765 P04A5 2C8F
0766
0766 P04A6 00EE
0766 P04A7 87FE
0766 P04A8 80BA
0767
0767 P04A9 4FFE
0767 P04AA 0FD2

                    CMA+ LOWER,FAD,AND,CST,TL1,EN,NU,$F0          SAVE PPPP0000

                    SEQ  UPPER,N1,S2,CST,FA,E1,CLRUDC,$1C         FA TO LMC

                    CMA+ LOWER,N1,S2,CST,L2F,EN,NU,LMCTF/N-S/N    SET LMC TO TF

                    SEQ  UPPER,L1,S1,NU,L2F,E1,INCFPA,NU,NU       STORE PPPP0000

                    CMA+ LOWER,NU,NU,NU,NONE,E1,STBCB1,SETRD,NU   SET DMA RD MODE

                    SEQ  UPPER,NU,NU,NU,NONE,EB,LOADFA,PLOUDC,$6  FA TO T-FWA-H

                    JPT+ UPPER,NU,NU,NU,NONE,EN,NU,DMASEQ         DO DMA RD

                    CMA+ LOWER,N1,S2,CST,FA,E1,CLRUDC,$1C         FA TO LMC

                    SEQ  UPPER,N1,S2,CST,L2F,EN,NU,LMCMF/N-S/N    SET LMC TO MF

                    CMA+ LOWER,L1,S1,NU,L2F,E1,INCFPA,NU,NU       STORE PORT

                    SEQ  UPPER,NU,NU,NU,NONE,E1,STBCB1,SETRD,NU   SET DMA RD MODE

                    CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLOUDC,$A  FA TO MS-FWA-H

                    JPT  UPPER,NU,NU,NU,NONE,EN,NU,DMASEQ         GO DO DMA RD
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0769                    MDMSCN CMA+ LOWER,N1,ONES,NU,FA,E2,NU,PLDUDC,$3     FA=FF,SEG3-NXT MDM
0769 P04AB 00EF
0769 P04AC 809E
0769 P04AD 0FB3
0770                        SEQ  AUEQFF,FLE,OR,CST,NONE,EN,NU,$F3           IS DELAY COMPL
0770 P04AE E20A
0770 P04AF 0FF3
0771                        SEQ+ UPPER,FLE,S1,NJ,FA,E1,LDPNR,NU,NU          DELAY COMPL
0771 P04B0 00F0
0771 P04B1 CA06
0771 P04B2 EFFF
0772                        JPT  UPPER,FLE,PLUS,BTG,L2F,E1,ARITHN,AQSCAN DELAY NOT COMPL-ADD4
0772 P04B3 4A37
0772 P04B4 E20B
0773                        CMA+ LOWER,NU,NU,NU,NONE,EB,LOADFA,PLDUDC,$01  FA OF FLAG R1
0773 P04B5 00F1
0773 P04B6 87FE
0773 P04B7 30B1
0774                        SEQ  AUEQFF,FLE,ORN,BTG,NONE,E2,BG7,PLDUDC,$3  IS PRT IN LBT MODE
0774 P04B8 E216
0774 P04B9 17B3
0775                        JPT+ LOWER,N1,ONES,NU,TL1,EN,NU,MDMNXT         PORT IN LBT MODE
0775 P04BA 00F2
0775 P04BB 409F
0775 P04BC 4FF8
0776                        SEQ  UPPER,NU,NU,NU,NONE,E2,NU,LDPCR,$1        PORT NOT IN LBT MODE
0776 P04BD CFFE
0776 P04BE 1FC1
0777                        CMA+ LOWER,NU,NU,NU,NONE,E2,NU,LDPCR,$5         CS-ST-RD
0777 P04BF 00F3
0777 P04C0 87FE
0777 P04C1 1FC5
0778                        SEQ  UPPER,NU,NU,NU,NONE,E1,LOADFA,$0E          NOP- FRA-E,SEG3
0778 P04C2 CFFE
0778 P04C3 200E
0779                        SEQ+ AUX1,PBXI,S1,NJ,TL2,E2,DSRSET,LDPCR,$0    DSR OR DCD SET
0779 P04C4 00F4
0779 P04C5 0407
0779 P04C6 98C0
0780                    MDMTST JPT  UPPER,FLE,EORZ,L2,TL1,EN,NU,NEWTFL      L1=FF IF NO MDM CHNG
0780 P04C7 4A31
0780 P04C8 4FF8
0781                        JPT+ AUX1,NU,NU,NU,NONE,EN,L2BIT7,DSRBIT        DSR SET
0781 P04C9 00F5
0781 P04CA 57FE
0781 P04CB 07F6
0782                        JPT  AUX1,NU,NU,NU,NONE,EN,L2BIT7,DCDBIT        DCD SET
0782 P04CC 57FE
0782 P04CD 07F7
0783                    DSRBIT JPT+ LOWER,FLE,OR,BTG,TL2,EN,BG2,MDMTST      DSR IS A 1
0783 P04CE 00F6
0783 P04CF 420F
0783 P04D0 82F4
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0784                        JPT  LOWER,FLE,ANDN,BTG,TL2,EN,BG2,MDMTST    DSR IS A 0
0784 P04D1 4247
0784 P04D2 82F4
0785                DCDBIT  JPT+ LOWER,FLE,OR,BTG,TL2,EN,BG1,MDMTST     DCD IS A 1
0785 P04D3 00F7
0785 P04D4 420F
0785 P04D5 81F4
0786                        JPT  LOWER,FLE,ANDN,BTG,TL2,EN,BG1,MDMTST    DCD IS A 0
0786 P04D6 4247
0786 P04D7 81F4
0787                NEWTFL  CMA+ LOWER,N1,S2,L2,L2F,EN,NU,NU,NU          UPDATE STATUS WORD
0787 P04D8 00F8
0787 P04D9 80A9
0787 P04DA CFFF
0788                MDMNXT  SEQ  AUEQFF,FAD,OR,OST,FA,EN,NU,$0F          IS THIS PORT F
0788 P04DB E38A
0788 P04DC CF0F
0789                        SEQ+ AUX1,NU,NU,NU,NONE,EN,DSRSET,NU,NU      YES PORT F
0789 P04DD 00F9
0789 P04DE 07FE
0789 P04DF 08FF
0790                        JPT  UPPER,N1,ONES,NU,FA,EN,NU,MDMINC        NOT PORT F, FA TO FF
0790 P04E0 489E
0790 P04E1 CFFB
0791                        SEQ+ UPPER,NU,NU,NU,NONE,E1,STBCB1,SELDCD,NU DSR SET,FLIP TO DCD
0791 P04E2 00FA
0791 P04E3 CFFE
0791 P04E4 2C2F
0792                        SEQ  UPPER,NU,NU,NU,NONE,E1,STBCB1,SELDSR,NU DCD SET,FLIP TO DSR
0792 P04E5 CFFE
0792 P04E6 2CAF
0793                MDMINC  CMA+ LOWER,FLE,PLUS,BTG,L2F,E1,ARITHN,NU,NU  INCR AND CLR DELAY
0793 P04E7 00FB
0793 P04E8 8237
0793 P04E9 E2FF
0794                        SEQ  AUX1,NU,NU,NU,NONE,EN,L2BIT0,NU,NU      TEST MIP BIT
0794 P04EA 07FE
0794 P04EB 06FF
0795                        SEQ+ AUEQFF,L1,S1,NU,NONE,E1,LOADFA,$0E      HERE-MIP ON-TST CHNG
0795 P04EC 00FC
0795 P04ED E086
0795 P04EE 200E
0796                        JPT  UPPER,NU,NU,NU,NONE,EN,NU,AQSCAN        HERE-MIP NOT ON
0796 P04EF 4FFE
0796 P04F0 0F03
0797                        JPT+ UPPER,NU,NU,NU,NONE,EN,NU,AQSCAN        HERE-L1=FF NO CHNG
0797 P04F1 00FD
0797 P04F2 4FFE
0797 P04F3 0F03
0798                        JPT  UPPER,FLE,OR,BTG,L2F,EN,BG6,STKSTW      HERE-SET MDM BIT
0798 P04F4 4A0F
0798 P04F5 C61D
0799                NIPTST  JPT+ LOWER,N1,ONES,NU,ATL,E1,RPLYAQ,INTOFF   HERE-NIP(FE=00)
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0799 P04F6 00FE
0799 P04F7 409E
0799 P04F8 AA0A
0800                    JPT   LOWER,NU,NU,NU,NONE,EN,NU,TSRSF        HERE-STACK FULL
0800 P04F9 47FE
0800 P04FA 0F22
0801              CHERJP JPT+ LOWER,NU,NU,NU,NONE,EN,NU,CERTST       HERE-NO JUMPER
0801 P04FB 00FF
0801 P04FC 47FE
0801 P04FD 0F42
0802                    JPT   UPPER,NU,NU,NU,NONE,EN,NU,NERTST       HERE-JUMPER IN
0802 P04FE 4FFE
0802 P04FF 0F44
0803                    END

PGM=  0500 (  1280)   COM = 0000 (     0)   DAT = 0000 (     0)
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E Q U I V A L E N C E S

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0063	RXRDYN	0007	(000007)	0306
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0130    E2      0001    (000001)        0285, 0296, 0298, 0304, 0308, 0330, 0333, 0334, 0335, 0354, 0355, 0359, 0373, 0378, 0380, 0381
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0131    E1      0002    (000002)        0281, 0284, 0286, 0288, 0289, 0290, 0291, 0292, 0293, 0294, 0297, 0299, 0300, 0302, 0305, 0306
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0132    EB      0003    (000003)        0282, 0283, 0287, 0295, 0307, 0329, 0357, 0362, 0365, 0369, 0376, 0386, 0387, 0388, 0399, 0401
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0136    NSCHER  0000    (000000)        0417
0137    T1PWAO  0001    (000001)
0138    PRIT2   0002    (000002)
0139    EXTT2   0003    (000003)
0140    PFNOT   0004    (000004)        0310
0141    READ    0005    (000005)        0308
0142    L2BIT6  0006    (000006)        0370, 0438, 0616, 0794
0143    L2BIT7  0007    (000007)        0533, 0781, 0782
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0144    DMAFLG  0008    (000008)    0385
0145    AQRDWT  0009    (000009)    0304
0146    SEGEQ3  000A    (000010)    0285, 0381
0147    DSRSET  000B    (000011)    0779, 0789
0148    TXRDY   000C    (000012)    0460
0149    NOTERR  000D    (000013)    0665
0150    MPF     000E    (000014)
0151    MAE     000F    (000015)    0671, 0679, 0694, 0734
0155    BG0     0000    (000000)    0351, 0375, 0415, 0434, 0462, 0508, 0553, 0617, 0636, 0637, 0661, 0662, 0670, 0675, 0687, 0739
0156    BG1     0001    (000001)    0349, 0393, 0406, 0474, 0476, 0490, 0556, 0624, 0646, 0753, 0785, 0786
0157    BG2     0002    (000002)    0317, 0371, 0405, 0431, 0437, 0451, 0498, 0499, 0579, 0592, 0666, 0706, 0735, 0783, 0784
0158    BG3     0003    (000003)    0314, 0471, 0500, 0516, 0518, 0559, 0598, 0622, 0630, 0640, 0663, 0712, 0737
0159    BG4     0004    (000004)    0301, 0466, 0485, 0486, 0588, 0615, 0642
0160    BG5     0005    (000005)    0448, 0470, 0552, 0585
0161    BG6     0006    (000006)    0541, 0798
0162    BG7     0007    (000007)    0333, 0373, 0391, 0435, 0436, 0459, 0484, 0538, 0678, 0774
0166    LOADFA  0000    (000000)    0308, 0368, 0387, 0388, 0401, 0403, 0409, 0412, 0418, 0421, 0429, 0430, 0432, 0443, 0445, 0447
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0167    CLRERR  0001    (000001)    0293, 0672, 0673, 0684, 0685, 0688, 0689, 0726, 0727
0168    ARITHN  0002    (000002)    0306, 0309, 0312, 0342, 0352, 0396, 0425, 0426, 0455, 0478, 0479, 0537, 0539, 0607, 0654, 0683
                                    0708, 0725, 0772, 0793
0169    ARITHC  0003    (000003)    0345, 0524, 0525, 0526, 0629, 0638, 0701, 0718, 0719, 0722, 0723
0170    INCFPA  0004    (000004)    0283, 0297, 0348, 0651, 0748, 0757, 0764
0171    INCTFA  0005    (000005)    0284, 0321, 0350, 0362, 0367, 0377, 0427, 0428, 0469, 0480, 0481, 0501, 0521, 0522, 0523, 0551
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0172    SFTL2R  0006    (000006)    0369, 0531
0173    SFTL2L  0007    (000007)    0305
0177    REQDMA  0008    (000008)    0724
0178    CLRDMA  0009    (000009)    0720, 0721
0179    RPLYAQ  000A    (000010)    0325, 0327, 0332, 0338, 0357, 0363, 0365, 0529, 0535, 0536, 0540, 0542, 0544, 0546, 0560, 0577
                                    0578, 0595, 0604, 0611, 0635, 0644, 0799
0180    RJCTAQ  000B    (000011)    0311, 0633
0181    STBCB1  000C    (000012)    0281, 0289, 0291, 0292, 0294, 0299, 0300, 0302, 0329, 0331, 0346, 0364, 0366, 0376, 0450, 0468
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                                    0791, 0792
0182    CLRUDC  000D    (000013)    0282, 0287, 0313, 0341, 0360, 0399, 0408, 0432, 0445, 0454, 0467, 0482, 0483, 0530, 0618, 0639
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0183    SETDMA  000E    (000014)    0290
0184    LDPNR   000F    (000015)    0285, 0288, 0295, 0307, 0386, 0456, 0656, 0667, 0677, 0693, 0699, 0732, 0733, 0771
0188    LDFA1   0000    (000000)
0189    LDDMAH  0001    (000001)    0710
0190    LDDTL   0002    (000002)    0696, 0743
0191    LDDTU   0003    (000003)    0697, 0744
0192    PEPNR   0004    (000004)    0386
0193    INCFA1  0005    (000005)
0194    LDDMAL  0006    (000006)    0716
0195    LDDMAU  0007    (000007)    0717
0199    ROMPG0  0008    (000008)
0200    ROMPG1  0009    (000009)
0201    SETTM   000A    (000010)    0283, 0355, 0373
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0202	PLDUDC	0003	(000011)	0304, 0357, 0381, 0388, 0413, 0415, 0416, 0421, 0424, 0443, 0447, 0449, 0464, 0488, 0507, 0515
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				0750, 0759, 0766, 0769, 0773, 0774
0203	LDPCR	000C	(000012)	0282, 0295, 0296, 0298, 0329, 0330, 0333, 0334, 0335, 0362, 0369, 0376, 0378, 0380, 0399, 0403
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				0513, 0566, 0567, 0569, 0619, 0620, 0622, 0776, 0777, 0779
0204	CNTDWN	000D	(000013)	0354, 0355, 0359, 0409, 0429, 0430, 0477, 0524, 0549, 0583, 0612, 0641, 0723, 0740, 0742
0205	CNTUP	000E	(000014)	0285, 0307, 0387, 0401, 0457, 0520, 0581, 0587, 0595, 0603, 0610, 0625, 0634
0206	RSTPEL	000F	(000015)	0287, 0397, 0422, 0435, 0440, 0492, 0680
0210	CLRRD	0001	(000000)	0700, 0749
0211	CLRPRT	0001	(000001)	
0212	SELDCD	0002	(000002)	0791
0213	MAB201	0003	(000003)	0715
0214	PRTDDS	0004	(000004)	0299, 0331, 0496, 0514, 0570, 0623
0215	MAB181	0005	(000005)	0713
0216	CLRBRG	0006	(000006)	0289, 0366
0217	CLRINT	0007	(000007)	0302
0218	SETRD	0008	(000008)	0758, 0765
0219	SETPRT	0009	(000009)	0300
0220	SELDSR	000A	(000010)	0792
0221	MAB200	000B	(000011)	0292, 0714
0222	PRTDEN	000C	(000012)	0294, 0450
0223	MAB180	000D	(000013)	0291, 0711
0224	SETBRG	000E	(000014)	0281, 0364
0225	SETINT	000F	(000015)	0346

S Y M B O L S

DEF.LINE	NAME	ADDRESS	REFERENCED AT LINE NUMBER
0281	S	0000	0281, 0283, 0285, 0286, 0287, 0288, 0289, 0291, 0293, 0295, 0297, 0297, 0299, 0301, 0301, 0303 0305, 0306, 0307, 0309, 0309, 0311, 0311, 0312, 0313, 0313, 0314, 0315, 0315, 0316, 0317, 0317 0318, 0319, 0319, 0320, 0321, 0321, 0322, 0323, 0323, 0324, 0325, 0325, 0326, 0327, 0327, 0328 0329, 0331, 0332, 0333, 0335, 0337, 0337, 0338, 0341, 0342, 0343, 0345, 0347, 0347, 0349, 0350 0351, 0351, 0353, 0355, 0357, 0359, 0360, 0362, 0363, 0363, 0364, 0366, 0368, 0370, 0371, 0372 0374, 0374, 0375, 0376, 0378, 0380, 0382, 0382, 0383, 0385, 0385, 0387, 0389, 0390, 0391, 0391 0392, 0393, 0393, 0395, 0395, 0397, 0398, 0399, 0401, 0403, 0405, 0405, 0407, 0407, 0409, 0411 0413, 0415, 0417, 0417, 0419, 0419, 0421, 0423, 0423, 0425, 0426, 0427, 0427, 0429, 0431, 0431 0433, 0433, 0435, 0436, 0437, 0438, 0439, 0439, 0441, 0441, 0442, 0443, 0445, 0447, 0448, 0449 0451, 0452, 0454, 0456, 0458, 0458, 0460, 0461, 0462, 0463, 0464, 0465, 0466, 0468, 0470, 0471 0472, 0472, 0474, 0476, 0476, 0478, 0479, 0480, 0480, 0482, 0484, 0486, 0487, 0488, 0490, 0490 0492, 0494, 0494, 0496, 0499, 0500, 0501, 0502, 0503, 0503, 0504, 0505, 0507, 0509, 0510, 0511 0513, 0515, 0516, 0517, 0518, 0520, 0522, 0524, 0525, 0526, 0526, 0527, 0528, 0529, 0530, 0532 0533, 0534, 0535, 0536, 0537, 0538, 0539, 0540, 0540, 0541, 0542, 0542, 0543, 0544, 0544, 0545 0546, 0546, 0547, 0549, 0551, 0553, 0553, 0554, 0555, 0556, 0557, 0559, 0559, 0560, 0561, 0563 0565, 0567, 0569, 0571, 0572, 0573, 0575, 0576, 0577, 0579, 0579, 0581, 0583, 0585, 0587, 0589 0591, 0592, 0593, 0595, 0596, 0597, 0599, 0600, 0601, 0603, 0605, 0606, 0607, 0607, 0609, 0609 0611, 0613, 0615, 0617, 0618, 0619, 0621, 0623, 0624, 0625, 0626, 0627, 0629, 0629, 0630, 0631 0631, 0633, 0633, 0635, 0635, 0636, 0637, 0639, 0640, 0641, 0642, 0643, 0645, 0646, 0648, 0649 0650, 0651, 0652, 0653, 0654, 0656, 0658, 0658, 0660, 0660, 0662, 0662, 0663, 0664, 0666, 0667 0668, 0668, 0670, 0670, 0672, 0674, 0675, 0676, 0678, 0679, 0680, 0681, 0682, 0683, 0684, 0686 0687, 0688, 0690, 0692, 0694, 0694, 0696, 0698, 0698, 0700, 0702, 0702, 0704, 0706, 0708, 0710 0712, 0714, 0716, 0718, 0720, 0720, 0722, 0724, 0724, 0725, 0726, 0728, 0730, 0731, 0732, 0734 0734, 0736, 0737, 0738, 0739, 0740, 0741, 0742, 0744, 0746, 0747, 0748, 0750, 0751, 0752, 0752 0754, 0756, 0756, 0758, 0760, 0760, 0762, 0763, 0764, 0766, 0767, 0769, 0771, 0772, 0773, 0775 0775, 0777, 0779, 0780, 0781, 0781, 0782, 0783, 0783, 0784, 0785, 0785, 0786, 0787, 0789, 0790 0791, 0793, 0795, 0796, 0797, 0797, 0798, 0799, 0799, 0800, 0801, 0801, 0802
0284	ZTF	0008	0286, 0288
0293	MCMODE	001E	0301
0295	NXTPRT	0023	0297
0302	INTOFF	0035	0799
0303	AQSCAN	0037	0311, 0327, 0332, 0337, 0347, 0360, 0395, 0433, 0442, 0487, 0494, 0504, 0510, 0518, 0535, 0554 0556, 0559, 0560, 0572, 0576, 0596, 0606, 0633, 0724, 0772, 0796, 0797
0313	AQJMT	0050	0309, 0312
0327	SPSTRD	0073	
0329	AQEC01	0078	0323
0333	CTSDSR	0082	0321, 0338
0341	STKSTW	0091	0683, 0739, 0798
0343	POST	0096	0342
0349	TSR	00A5	0313, 0351
0352	TSRSF	00AD	0800

0362	PRTMDS	00C3	0314
0371	SETDLY	00DA	0374, 0383
0375	SETMIP	00E4	0382
0377	DELAY	00E9	0371
0385	RXRDY1	00FA	0306
0390	EOTHI	0107	0391
0393	EOTLT	010E	0325, 0398
0397	EOTCMP	0118	0390
0399	RDURT	011D	0642
0408	RXSTAT	0134	0439
0418	GERTST	014D	0801
0421	NERTST	0154	0802
0424	RLENAD	015C	0436
0425	CTDNRL	015E	0427
0430	EOTCK	016B	0426
0431	EOTRLT	016D	0393, 0419
0435	EOTFLG	0177	0423
0437	ECOFLG	017C	0407
0441	RLZTRM	0186	0579
0442	RXTERM	0189	0431
0449	RCVDIS	019A	0405
0454	TXRDY1	01A4	0649, 0658
0458	TLZX	01AE	0646
0467	RXTXIT	01C5	0448
0471	INSLF1	01CF	0476
0479	TBRRW	01E3	0480
0483	FLPTUL	01ED	0472, 0479
0487	CRLFXT	01F7	0553
0488	FLGTFL	01F9	0490
0491	DOTMT	0201	0471, 0502
0492	RCVOFF	0203	0452
0494	TROFF3	0208	0375, 0438
0498	ECOTMT	0210	0465
0503	TROFF1	021C	0500
0505	TROFF2	0221	0461
0515	TRTRM1	023A	0458
0517	ECPXOF	023F	0503, 0626, 0640
0520	RBCNT	0244	0315
0521	TBCNT	0247	0317
0525	UBCSUB	0251	0526, 0527
0528	EXTSWR	0258	0319
0530	SUBFUN	0250	0322
0536	SFXFM	026C	0533
0540	SFJT	0276	0537, 0539
0549	CRLFPF	028A	0540
0554	ZTXSW	0297	0529
0555	INSTLF	0299	0542
0557	ECPLOF	029E	0544
0560	RPLAQS	02A6	0525
0561	ECPLON	02A8	0546
0564	PRTCMD	02B0	0541
0566	CMDSEQ	02B5	0592
0571	RFWAH	02C1	0543

0573	TFWAH	02C6	0545
0575	MFWAH	02C3	0547
0577	RLEN	02D0	0324
0593	RFWA16	02F8	0316
0594	FWASEQ	02FB	0600
0597	MFWA16	0302	0320
0601	TFWA16	030C	0318
0607	TSTTLU	0313	0609
0609	TLEN	0320	0326
0617	TXENBT	0334	0624
0624	TLOMAR	0346	0618
0629	RNDUPL	0352	0635
0630	CLONAY	0355	0737
0631	MLEN	0357	0328
0633	MLENA	035C	0631
0636	MOETST	0364	0392
0637	RNDUPU	0366	0629
0641	OESTAT	0370	0636
0644	TLENZ	0378	0607
0648	DMAFL1	037F	0385
0651	DPRTFA	0387	0653
0652	NXTRQS	0389	0670, 0681, 0741
0660	DOBMVF	039D	0752
0664	GETPRT	03A7	0651
0666	LMCTF	03AC	0675, 0756
0669	LMCTFX	03B4	0731
0671	TFME	03B9	0667
0676	LMCRS	03C5	0687, 0747
0680	RCVEND	03CF	0441
0682	TOSTSW	03D4	0516
0684	RSME	03D9	0679
0688	MFME	03E3	0694
0692	LMCMF	03E0	0763
0698	MSDMA	03FC	
0708	MSBRRW	0415	0702
0710	DMASEQ	041A	0751, 0760, 0767
0723	FWAHP1	0438	0725
0724	DMAREQ	043D	0720
0726	MSME	0442	0734
0731	STORUP	044F	0668
0732	LMCMS	0451	0698
0740	RQBMVF	0465	0630
0742	RSDMA	046A	0662
0752	TFDMA	0483	0663
0761	MFDMA	049A	0660
0769	MDMSCN	04AB	0463
0780	MDMTST	04C7	0783, 0784, 0785, 0786
0783	DSRBIT	04CE	0781
0785	DCDBIT	04D3	0782
0787	NEWTFL	04D8	0780
0788	MDMNXT	04DB	0775
0793	MDMINC	04E7	0790
0799	NIPTST	04F6	0350

0801 CHERJP 04F8 0417

*** A L P H A B E T I C A L S O R T O F S Y M B O L S ***

AND	0084	ANDN	0088	AOEC01	0329	AQJMT	0313	AQROWT	0145	AQSCAN	0303	ARITHC	0169	ARITHN	0168	ATL	0120
ATU	0119	AUEQFF	0060	AUX1	0058	BG0	0155	BG1	0156	BG2	0157	BG3	0158	BG4	0159	BG5	0160
BG6	0161	BG7	0162	BTG	0114	CERTST	0418	CHERJP	0801	CLDNAY	0630	CLRBRG	0216	CLRDMA	0178	CLRERR	0167
CLRINT	0217	CLRPRT	0211	CLRRD	0210	CLRUDC	0182	CMDSEQ	0566	CNTDWN	0204	CNTUP	0205	CRLFPF	0549	CRLFXT	0487
CST	0112	CTDNRL	0425	CTSDSR	0333	CYNOT	0062	DCDBIT	0785	DELAY	0377	DFL	0069	DFU	0070	DMAFL1	0648
DMAFLG	0144	DMAREQ	0724	DMASEQ	0710	DOBMVF	0660	DOTMT	0491	DPRTFA	0651	DSRBIT	0783	DSRSET	0147	E1	0131
E2	0130	E8	0132	ECOFLG	0437	ECOTMT	0498	ECPLOF	0557	ECPLON	0561	ECPXOE	0517	EN	0129	EOR	0089
EORZ	0086	EOTCK	0430	EOTCMP	0397	EOTFLG	0435	EOTHI	0390	EOTLT	0393	EOTRLT	0431	EXTSWR	0528	EXTT2	0139
FA	0121	FAD	0074	FLE	0071	FLGTFL	0488	FLPTUL	0483	FPAEQF	0061	FRAEQE	0059	FWAHP1	0723	FWASEQ	0594
GETPRT	0664	I	0000	INCFA1	0193	INCFPA	0170	INCTFA	0171	INSLF1	0471	INSTLF	0555	INTOFF	0302	L1	0068
L2	0111	L2BIT0	0142	L2BIT7	0143	L2F	0125	LDDMAH	0189	LDDMAL	0194	LDDMAU	0195	LDDTL	0190	LDDTU	0191
LDFA1	0188	LDPCR	0203	LDPNR	0184	LMCMF	0692	LMCMS	0732	LMCRS	0676	LMCTF	0666	LMCTFX	0669	LOADFA	0166
LOWER	0056	MAB180	0223	MAB181	0215	MAB200	0221	MAB201	0213	MAE	0151	MCMODE	0293	MDMINC	0793	MDMNXT	0788
MDMSCN	0769	MDMTST	0780	MFDMA	0761	MFME	0688	MFWA16	0597	MFWAH	0575	MINUS	0106	MINUS1	0099	MLEN	0631
MLENA	0633	MOETST	0636	MPF	0150	MSBRRW	0708	MSDMA	0698	MSME	0726	N	0052	N1	0067	NAL	0073
NAND	0091	NAU	0072	NERTST	0421	NEWTFL	0787	NIPTST	0799	NONE	0118	NOR	0087	NOTERR	0149	NS1AND	0093
NSCHER	0136	NU	0079	NXTPRT	0295	NXTRQS	0652	OESTAT	0641	ONES	0083	OR	0081	ORN	0082	ORZ	0094
P8XI	0075	PEPNR	0192	PLDUDC	0202	PLUS	0101	PLUS1	0107	PORTDL	0122	POST	0343	PPNOT	0140	PRIT2	0138
PRTCMD	0564	PRTDDS	0214	PRTDEN	0222	PRTMDS	0362	PS2P1	0105	QFL	0113	RBCNT	0520	RCVDIS	0449	RCVEND	0680
RCVOFF	0492	RDURT	0399	READ	0141	REQDMA	0177	RFWA16	0593	RFWAH	0571	RJCTAQ	0180	RLEN	0577	RLENAD	0424
RLZTRM	0441	RNDUPL	0629	RNDUPU	0637	ROMPG0	0199	ROMPG1	0200	RPLAQS	0560	RPLYAQ	0179	RQBMVF	0740	RSOMA	0742
RSME	0684	RSTPEL	0206	RXRDY1	0385	RXRDYN	0063	RXSTAT	0408	RXTERM	0442	RXTXIT	0467	S	0281	S1	0080
S1Z	0095	S2	0085	S2Z	0090	SEGEQ3	0146	SELDCD	0212	SELDSR	0220	SETBRG	0224	SETDLY	0371	SETDMA	0183
SETINT	0225	SETMIP	0375	SETPRT	0219	SETRD	0218	SETTM	0201	SFJT	0540	SFTL2L	0173	SFTL2R	0172	SFXFM	0536
SHIFT	0100	SPSTRD	0327	STBCB1	0181	STKSTW	0341	STORUP	0731	SUBFUN	0530	T1PWAO	0137	TBCNT	0521	TBRRW	0479
TFDMA	0752	TFME	0671	TFWA16	0601	TFWAH	0573	TL1	0123	TL2	0124	TLDMAR	0624	TLEN	0609	TLENZ	0644
TLZX	0458	TOSTSW	0682	TROFF1	0503	TROFF2	0505	TROFF3	0494	TRTRM1	0515	TSR	0349	TSRSF	0352	TSTTLU	0607
TXENBT	0617	TXRDY	0148	TXRDY1	0454	UBCSUB	0525	UPPER	0057	ZERO	0092	ZTF	0284	ZTXSW	0554		

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CDC® DT610, DY221, FJ127, FJ128
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Hardware Reference/Maintenance Manual

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